# FSC-WF1101FJ

DATASHEET V1.0

# 1 INTRODUCTION

## Overview

FSC-WF1101FJ is a small size and low profile of Wi-Fi 6 module, board size is 12*15mm, It can be easily manufactured on SMT process and highly suitable for tablet PC, mobile device and consumer products, It provides SDIO 2.0 interface for Wi-Fi to connect with host processor

FSC-WF1101FJ offers Wi-Fi 6 while maintaining compatibility with Wi-Fi 4 (802.11 a/b/g/n) and Wi-Fi 5 (802.11ac)

## Features

- 2.4GHz and 5GHz, 20MHz, single spatial stream
- MAC, baseband, and RF transceiver with support for IEEE 802.11 a/b/g/n/ax
- Hardware-based encryption and decryption supporting WPA2 and WPA3
- Excellent interoperability
- Application throughput up to 50Mbps
- Companion IC to any processor or MCU host capable of running a TCP/IP stack
- solution with up to +20.5dBm output power.

## Application

- Grid infrastructure
- Building and home automation
- Appliances
- Medical
- Retail automation and payment
- Printers

# 2 General Specification

Table 2- 1： General Specifications

| Categories | Features | Implementation |
|---|---|---|
| Wi-Fi | | |
| | WLAN Standard | IEEE 802.11 a/b/g/n/ax Wi-Fi compliant |
| | Frequency Range | 2.400 GHz~2.4835 GHz (2.4 GHz ISM Band)<br>5.150 GHz5.850 GHz (5.0 GHz Band) |
| | Transmit Power | UP TO 20.5 dBm |
| | Receiver | -91dBm（6 Mbps OFDM ） |
| | Interface | SDIO/SPI |
| Size | | 12mm × 15 mm × 2.4mm |
| Operating temperature | | -40°C ~+105°C, |
| Storage temperature | | -40°C ~+105°C |
| Supply Voltage | | 1.8V |
| Miscellaneous | Lead Free<br>Warranty | Lead-free and RoHS compliant<br>One Year |
| MSL grade: | | MSL 3 |
| ESD grade: | | Human Body Model: Pass ±2000 V,<br>Charge device model: Pass ±500 V, |

# 3 HARDWARE SPECIFICATION

## 3.1 Block Diagram and PIN Diagram

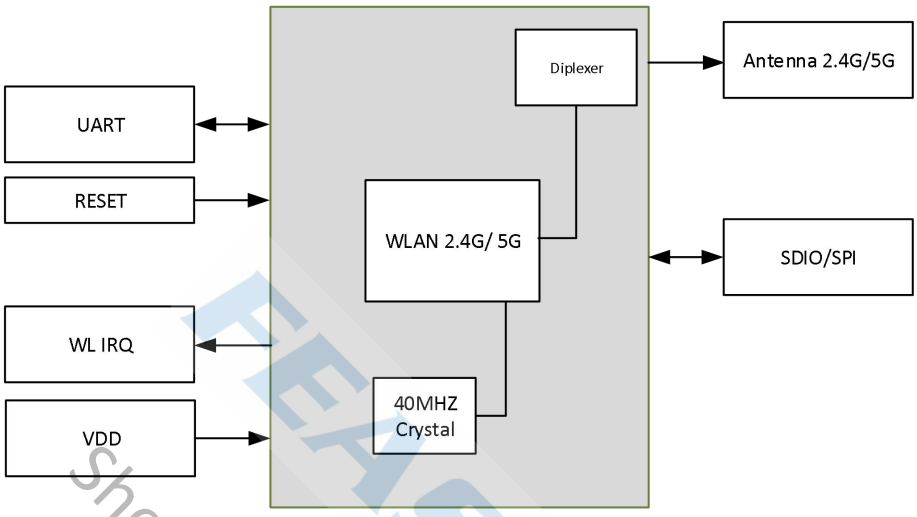



Figure 3- 1:Block Diagram

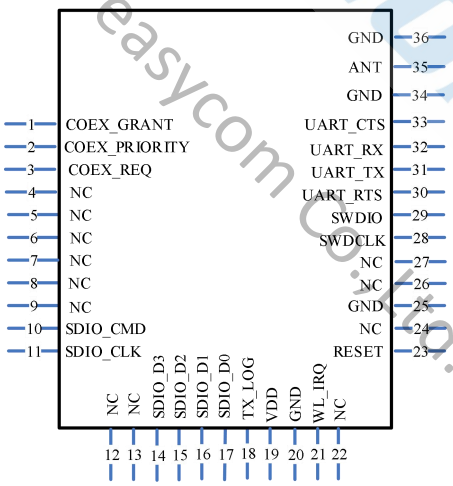



Figure 3- 2:FSC-WF1101FJ PIN Diagram(Top View)

## 3.2 PIN Definition Descriptions

Table 3- 2： Pin definition

| Pin | Pin Name | Type | Pin Descriptions | Notes |
|---|---|---|---|---|
| 1 | COEX_GRANT | O | External coexistence interface - grant | |
| 2 | COEX_PRIORITY | I | External coexistenceinterface - priority | |
| 3 | COEX_REQ | I | Extermal coexistence interface - request | |
| 4 | NC | | | |
| 5 | NC | | | |
| 6 | NC | | | |
| 7 | NC | | | |
| 8 | NC | | | |
| 9 | NC | | | |
| 10 | SDIO_CMD | I/O | SDIO command of SPI PICO | |
| 11 | SDIO_CLK | I | SDIO clock or SPI clock | |
| 12 | NC | | | |
| 13 | NC | | | |
| 14 | SDIO_D3 | I/O | SDIO data D3 or SPI CS | |
| 15 | SDIO_D2 | I/O | SDIO data D2 | |
| 16 | SDIO_D1 | I/O | SDIO data D1 | |
| 17 | SDIO_D0 | I/O | SDIO data DO or SPI POCI | |
| 18 | TX_LOG | I/O | Tracer (UART TX debug logger) | |
| 19 | VDD | VDD | 1V8 | |
| 20 | GND | Vss | Power Ground | |
| 21 | WL_IRQ | O | Interrupt request to host for WLAN | |
| 22 | NC | | | |
| 23 | RESET | I | RESET Active low | |
| 24 | NC | | | |
| 25 | GND | Vss | Power Ground | |
| 26 | NC | | | |
| 27 | NC | | | |
| 28 | SWDCLK | I | Serial wire debug clock | |
| 29 | SWDIO | I/O | Serial wire debug I/O | |
| 30 | UART_RTS | O | Device RTS signal - flow control | |

| | | | |
|---|---|---|---|
| 31 | UART_TX | O | UART Data output |
| 32 | UART_RX | I | UART Data input |
| 33 | UART_CTS | I | Device CTS signal flow control |
| 34 | GND | Vss | Power Ground |
| 35 | ANT | RF | WLAN 2.4GHz /5G RF port |
| 36 | GND | Vss | Power Ground |

# 4 MSL & ESD

Table 6- 1: MSL and ESD

| Parameter | Value |
|---|---|
| MSL grade: | MSL 3 |
| ESD grade | Electrostatic discharge |
| ESD – Human-body model (HBM) rating, JESD22-A114-F<br>(Total samples from one wafer lot) | Pass ±2000 V, all pins |
| ESD – Charge-device model (CDM) rating, JESD22-C101-D<br>(Total samples from one wafer lot) | Pass ±500 V, all pins |

# 5 RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below and follow instructions specified by IPC/JEDEC J-STD-033.

**Note:** The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

*Notice (注意) :*

*Feasycom module must use Step-Stencil, suggestion using the stencil thickness about 0.16-0.2mm,it could be modify with the product.*

Table 7- 1: Recommended baking times and temperatures

| MSL | 125°C Baking Temp. | | 90°C/≤ 5%RH Baking Temp. | | 40°C/ ≤ 5%RH Baking Temp. | |
|---|---|---|---|---|---|---|
| | Saturated @ 30°C/85% | Floor Life Limit + 72 hours @ 30°C/60% | Saturated @ 30°C/85% | Floor Life Limit + 72 hours @ 30°C/60% | Saturated @ 30°C/85% | Floor Life Limit + 72 hours @ 30°C/60% |
| 3 | 9 hours | 7 hours | 33 hours | 23 hours | 13 days | 9 days |

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

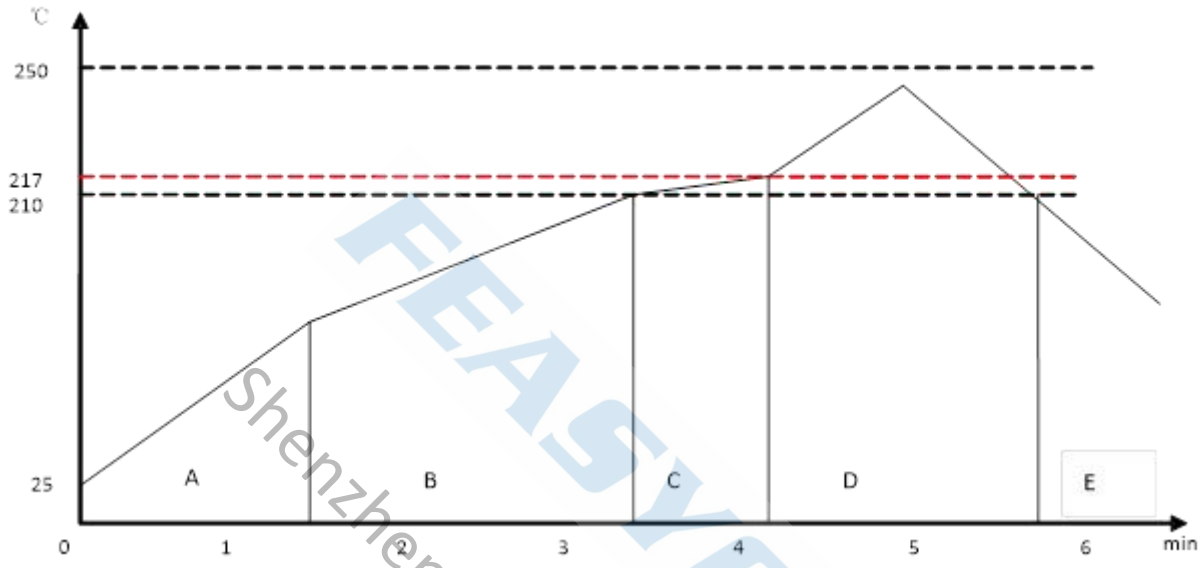



Figure 7-1, Typical Lead-free Re-flow

**Pre-heat zone (A)** — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

**Equilibrium Zone 1 (B)** — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

**Equilibrium Zone 2 (C) (optional)** — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

**Reflow Zone (D)** — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

**Cooling Zone (E)** — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

# 6 MECHANICAL DETAILS

## 6.1 Mechanical Details

- Dimension: 12mm(W) x 15mm(L) x 2.4mm(H) Tolerance: ±0.2mm
- Module size: 12mm X 15mm Tolerance: ±0.2mm
- Pad size: 1.7mmX0.5mm Tolerance: ±0.2mm
- Pad pitch: 0.9mm Tolerance: ±0.1mm

**(Residual plate edge error: < 0.5mm)**

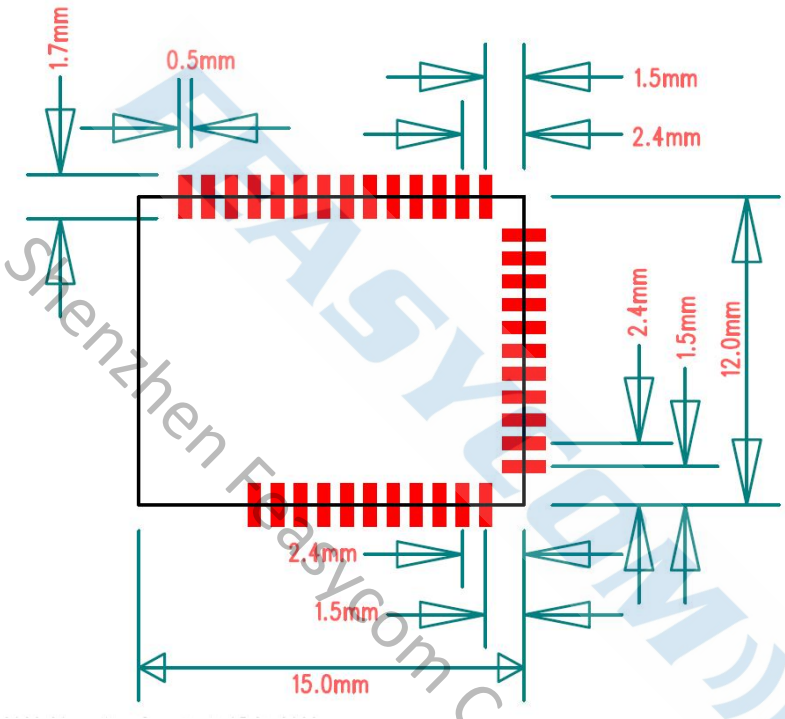



Figure 8- 1： FSC-WF1101FJ footprint Layout Guide (Top View)



# 7 HARDWARE INTEGRATION SUGGESTIONS

## 7.1 Soldering Recommendations

FSC-WF1101FJ is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

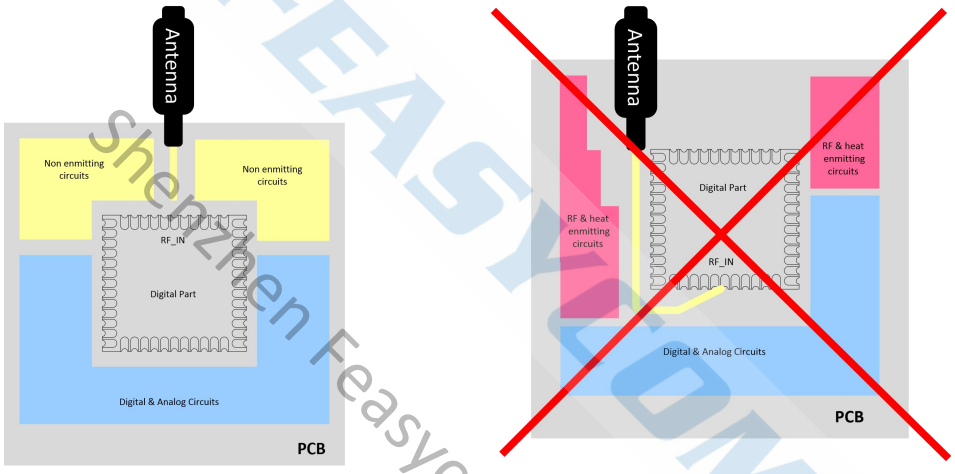
Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and

operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

## 7.2 Layout Guidelines(External Antenna)

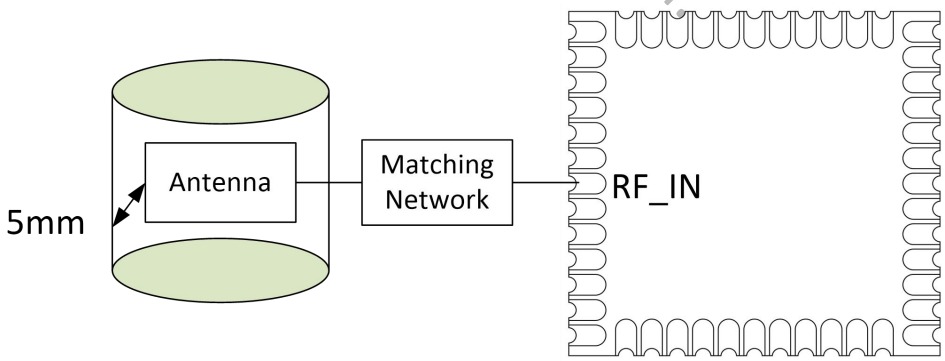
Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed




in this way that module digital part towards your digital section of the system PCB.

Figure 9- 3: Placement the Module on a System Board




### 7.2.1 Antenna Connection and Grounding Plane Design

Figure 9- 31-0: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

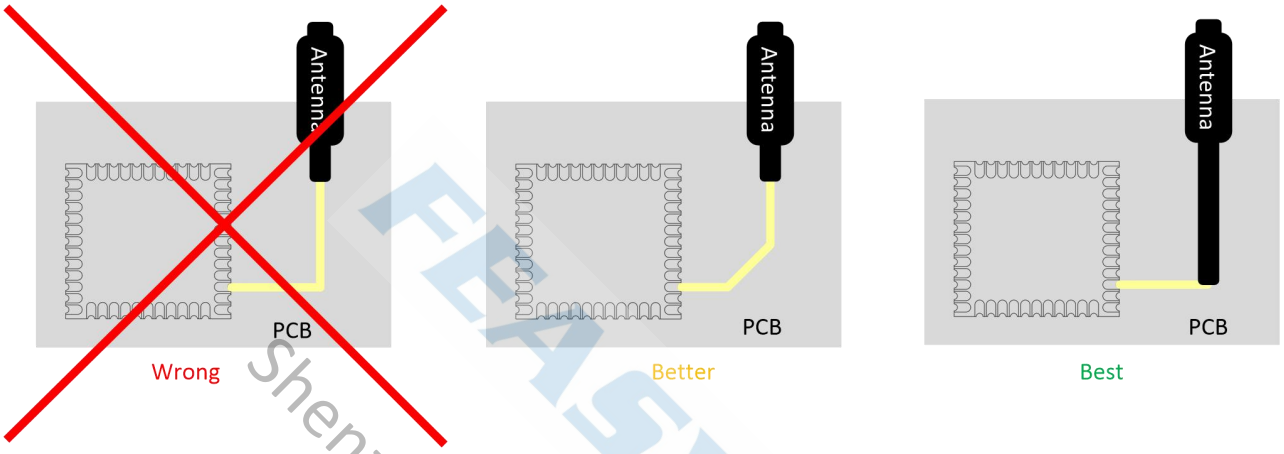



Figure 9- 31-1. Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many via as possible to connect the ground planes.

# 8 PRODUCT PACKAGING INFORMATION

## 8.1 Default Packing

Figure 10- 1: Tray Dimension: 140mm * 265mm Tray vacuum

## 8.2 Packing box(Optional)

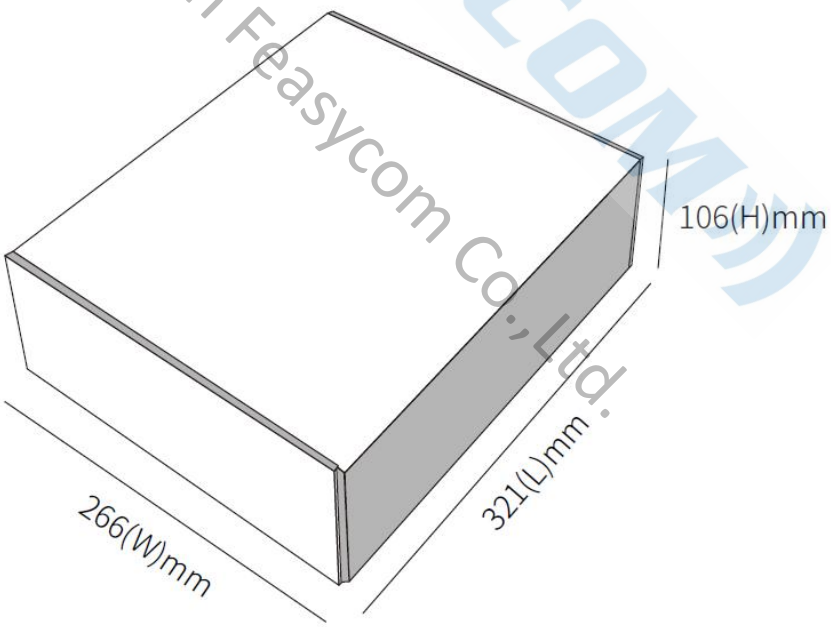



Figure 10- 2: Packing box(Optional)