FSC-BW2231

DATASHEET V1.2

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Revision History

Version	Data	Notes	Author
V1.0	2023-07-24	Initial Version	Devin Wan
V1.1	2023-09-12	1.Update PCM pin description - This pin should not pull high during power on module. 2.Modify the application circuit diagram(remove pull-up resistance of PCM pins) , And update some other error descriptions.	Devin Wan
V1.2	2024-08-30	Improve power consumption test items	Qiu

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1 INTRODUCTION

Overview

FSC-BW2231 is a small size and low profile of Wi-Fi + BT Combo module with LGA module, board size is 12*15mm. It can be easily manufactured on SMT process and highly suitable for tablet PC, mobile device and consumer products. It provides SDIO 2.0 interface for Wi-Fi to connect with host processor and high speed UART interface for BT5.2. It also has a PCM interface for audio data transmission with direct link to external audio codec via BT controller.

The Wi-Fi throughput up to 150Mbps in theory by using 802.11n technology.

General Features

- Operate at 2.4G&5GHz frequency bands
- 802.11 a/b/g/n + Bluetooth V2.1+EDR and BT5.2
- Enterprise level security which can apply WPA/WPA2/WPA3
- Wi-Fi 1T1R allow data rates supporting up to 150 Mbps PHY rates

Host Interface

- SDIO2.0 for Wi-Fi and UART for BT5.2
- PCM interface for audio data transmission via BT controller

Bluetooth Features

- Compatible with Bluetooth v2.1+EDR and V5.2 system
- Support BLE4.0, BT5.2 dual mode

Application

- Audio and video system
- Measurement systems
- PND

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2 General Specification

Table 2-1： General Specifications

Categories	Features	Implementation	
	Model Name	FSC-BW2231	
	Product Description	Support Wi-Fi/Bluetooth functionalities	
	Dimension	W x L x H: 12 x 12 x2.3 mm(typical)	
	Wi-Fi Interface	Support SDIO V1.1/2.0	
	BT Interface	UART / PCM	
	OS supported	Android /Linux/ Win CE /iOS /XP/WIN7/WIN10	
	Operating temperature	-40°C ~ +85°C	
	Storage temperature	-40°C ~ +85°C	
	Supply Voltage	3.0V~3.6V (Peak Current:500mA)	
	VDD_IO	1.62V~3.6V (Peak Current:100mA)	
	Miscellaneous	Lead-free and RoHS compliant Warranty - One Year	
	Humidity	10% ~ 90% non-condensing	
	MSL grade:	MSL 3	
	ESD grade:	Human Body Model: Pass ±3500 V, all pins Charge device model: Pass ±500 V, all pins	
Bluetooth			
	Bluetooth Standard	Bluetooth V5.2	
	Frequency Band	2402MHz ~ 2480MHz	
	Interface	UART/PCM	
	Modulation	GFSK, π /4-DQPSK, 8-DPSK	
	Transmit Power	+8 dBm (Max.)	
	Antenna Reference	Small antennas with 0~2dBi peak gain	
	Number of Channels	79 channels	
	Receiver	Sensitivity @ BER=0.1% for GFSK (1Mbps)	-92dBm
		Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)	-86dBm
		Sensitivity @ BER=0.01% for 8DPSK (3Mbps)	-85dBm
	Maximum Input Level	GFSK (1Mbps): -20dBm π/4-DQPSK (2Mbps) : -20dBm	
Wi-Fi 2.4GHz			
	WLAN Standard	IEEE 802.11 b/g/n Wi-Fi compliant	
	Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)	
	Number of Channels	2.4GHz： Ch1 ~ Ch14	
	Output Power	802.11b /11Mbps : 17dBm ± 2 dB EVM≤-9dB 802.11g /54Mbps : 15dBm ± 2 dB EVM≤-25dB	

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		802.11n /MCS7: 14dBm ± 2 dB EVM≤-28dB
	Spectrum Mask	Meet with IEEE standard
	Freq. Tolerance	±20ppm
	SISO Receive Sensitivity (11b,20MHz) @8% PER	1Mbps PER @ -92dBm EVM≤-83 2Mbps PER @ -90dBm EVM≤-80 5.5Mbps PER @ -87dBm EVM≤-79 11Mbps PER @ -85dBm EVM≤-76
	SISO Receive Sensitivity (11g,20MHz) @10% PER	6Mbps PER @ -89dBm EVM≤-85 9Mbps PER @ -88dBm EVM≤-84 12Mbps PER @ -87dBm EVM≤-82 18Mbps PER @ -84dBm EVM≤-80 24Mbps PER @ -81dBm EVM≤-77 36Mbps PER @ -78dBm EVM≤-73 48Mbps PER @ -73dBm EVM≤-69 54Mbps PER @ -71dBm EVM≤-68
	SISO Receive Sensitivity (11n,20MHz) @10% PER	MCS=0 PER @ -89dBm EVM≤-85 MCS=1 PER @ -86dBm EVM≤-82 MCS=2 PER @ -84dBm EVM≤-80 MCS=3 PER @ -80dBm EVM≤-77 MCS=4 PER @ -77dBm EVM≤-73 MCS=5 PER @ -72dBm EVM≤-69 MCS=6 PER @ -71dBm EVM≤-68 MCS=7 PER @ -69dBm EVM≤-67
	SISO Receive Sensitivity (11n,40MHz) @10% PER	MCS=0 PER @ -88dBm EVM≤-82 MCS=1 PER @ -85dBm EVM≤-79 MCS=2 PER @ -83dBm EVM≤-77 MCS=3 PER @ -79dBm EVM≤-74 MCS=4 PER @ -76dBm EVM≤-70 MCS=5 PER @ -71dBm EVM≤-66 MCS=6 PER @ -70dBm EVM≤-65 MCS=7 PER @ -68dBm EVM≤-64
	Maximum Input Level	802.11b : -10dBm 802.11g/n : -20dBm
	Antenna Reference	Small antennas with 0~2dBi peak gain
Wi-Fi 5GHz		
	WLAN Standard	IEEE 802.11a/n Wi-Fi compliant
	Frequency Range	5.150 GHz ~ 5.850 GHz (5.0 GHz Band)
	Number of Channels	5.0GHz： 36,40,44,48; 52,56,60,64; 100,104,108,112,116,120,124,128,132,136,140; 149,153,157,161,165.
	Output Power	802.11a/54Mbps: 15dBm ± 2dB EVM≤-25dB 802.11n /MCS7: 14dBm ± 2 dB EVM≤-28dB

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SISO Receive Sensitivity (11a,20MHz) @10% PER	6Mbps	PER @ -88dBm	EVM⩽-85
	9Mbps	PER @ -87dBm	EVM⩽-84
	12Mbps	PER @ -86dBm	EVM⩽-82
	18Mbps	PER @ -83dBm	EVM⩽-80
	24Mbps	PER @ -80dBm	EVM⩽-77
	36Mbps	PER @ -77dBm	EVM⩽-73
	48Mbps	PER @ -72dBm	EVM⩽-69
	54Mbps	PER @ -70dBm	EVM⩽-68
SISO Receive Sensitivity (11n,20MHz) @10% PER	MCS=0	PER @ -88dBm	EVM⩽-85
	MCS=1	PER @ -85dBm	EVM⩽-82
	MCS=2	PER @ -83dBm	EVM⩽-80
	MCS=3	PER @ -80dBm	EVM⩽-77
	MCS=4	PER @ -76dBm	EVM⩽-73
	MCS=5	PER @ -71dBm	EVM⩽-69
	MCS=6	PER @ -70dBm	EVM⩽-68
	MCS=7	PER @ -69dBm	EVM⩽-67
SISO Receive Sensitivity (11n,40MHz) @10% PER	MCS=0	PER @ -85dBm	EVM⩽-82
	MCS=1	PER @ -82dBm	EVM⩽-79
	MCS=2	PER @ -80dBm	EVM⩽-77
	MCS=3	PER @ -77dBm	EVM⩽-74
	MCS=4	PER @ -73dBm	EVM⩽-70
	MCS=5	PER @ -69dBm	EVM⩽-66
	MCS=6	PER @ -68dBm	EVM⩽-65
	MCS=7	PER @ -67dBm	EVM⩽-64
Maximum Input Level	802.11a/n : -30dBm		
Antenna Reference	Small antennas with 0~2dBi peak gain		

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3 HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

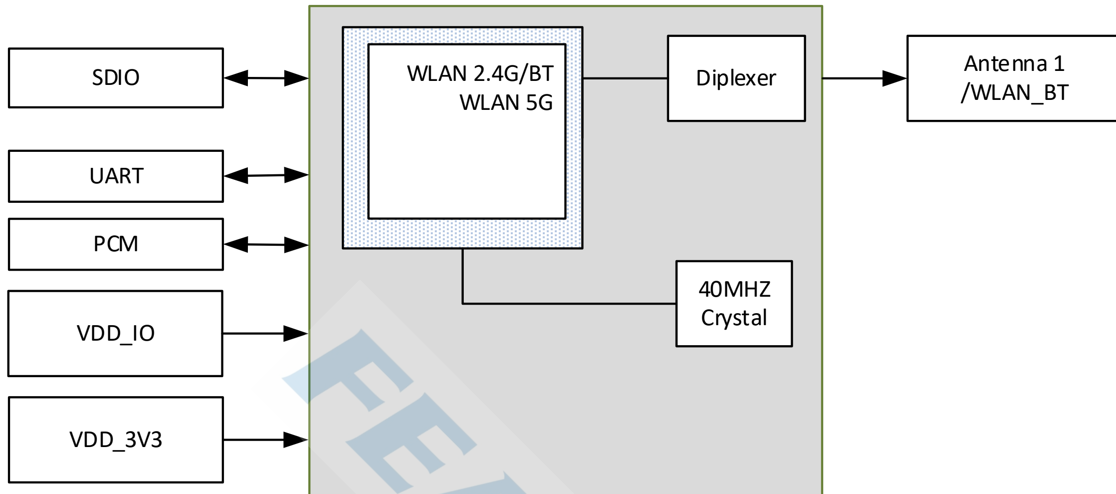

Figure 3-1-1: FSC-BW2231 Block Diagram

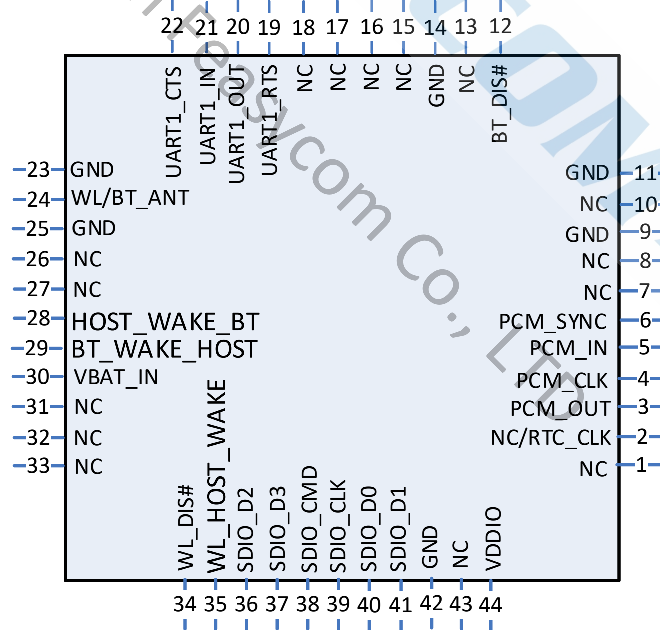

Figure 3-1-2: FSC-BW2231 PIN Diagram (Top View)

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3.2 PIN Definition Descriptions

Table 3-2-1: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	NC		Floating(NC)	
2	NC/RTC_CLK		External 32K or RTC clock	
3	PCM_OUT	O	PCM Output This pin should not pull high during power on module (此引脚在模块上电时不可拉高)	
4	PCM_CLK	I/O	PCM Clock	
5	PCM_IN	I	PCM Input This pin should not pull high during power on module (此引脚在模块上电时不可拉高)	
6	PCM_SYNC	O	PCM Sync, default low This pin should not pull high during power on module (此引脚在模块上电时不可拉高)	
7	NC		Floating (NC)	
8	NC		Floating (NC)	
9	GND		Ground connections	
10	NC/BT_ANT		Floating (NC)	
11	GND		Ground connections	
12	BT_DIS#	I	BT Reset IN	
13	NC		Floating (NC)	
14	GND		Ground connections	
15	NC		Floating (NC)	
16	NC		Floating (NC)	
17	NC		Floating (NC)	
18	NC		Floating (NC)	
19	UART_RTS		UART RTS Module pin is Ground connections	
20	UART_OUT	O	UART Output	
21	UART_IN	I	UART Input	
22	PCM_CTS	I	UART CTS	
23	GND		Ground connections	
24	WL/BT_ANT	I/O	WL/BT port for single antenna type(2.4G & 5G)(Figure 3-2-3)	
25	GND		Ground connections	
26	NC		Floating (NC)	
27	NC		Floating (NC)	
28	HOST_WAKE_BT	I	Host to wake up Bluetooth device	
29	BT_WAKE_HOST	O	Bluetooth device to wake up host	
30	VBAT_IN	P	3.3V±10% Main power voltage source input	

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31	NC		Floating (NC)
32	NC		Floating (NC)
33	NC		Floating (NC)
34	WL_DIS#	I	This pin pull low can externally shut down the WLAN function. (may not supported recently)
35	WL_HOST_WAKE	O	WLAN to wake up HOST
36	SD_D2	I/O	SDIO data line 2
37	SD_D3	I/O	SDIO data line 3
38	SD_CMD	I/O	SDIO command line
39	SDIO_CLK	I	SDIO clock line
40	SDIO_D0	I/O	SDIO data line 0
41	SDIO_D1	I/O	SDIO data line 1
42	GND		Ground connections
43	NC		Floating(NC)
44	VDDIO	P	I/O Voltage supply input

4 ELECTRICAL CHARACTERISTICS

4.1 DC Characteristic

Table 4-1-1: Power Supply Characteristics

Parameter	Min	Type	Max	Unit
Operating Temperature	-40	25	85	°C
VDD_3V3	3.0	3.3	3.6	V
VDD_IO	1.62	1.8 or 3.3	3.6	V

4.2 Power Supply DC Characteristics

Table 4-2-1: Power Consumption

Symbol	Parameter	Min	Type	Max	Unit
Power Consumption	TX HT40 11n Mode	/	106	/	mA
	TX HT20 11n Mode	/	122	/	mA
	TX HT20 11g Mode	/	126	/	mA
	TX HT20 11b Mode	/	265	/	mA
	RX Mode	/	69	/	mA
	Connect to 2.4G WiFi hotspot to test throughput and connect to Bluetooth	14	67	181.8	mA

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	Connect to 5G WiFi hotspot to test throughput and connect to Bluetooth	15	56	118.	mA
	Playing music while testing throughput on a 2.4G WiFi hotspot	68	168.8	318.69	mA
	Playing music while testing throughput on a 5G WiFi hotspot	71	204.11	405	mA

5 PHYSICAL INTERFACE

5.1 SDIO Interface Timing Specification

5.1.1 SDIO Interface Signal Levels

The module supports SDIO version 2.0 for all 1.8V / 3.3V . The host provides the power source with the target power level to the VDDIO pin.

5.1.2 SDIO Bus Times

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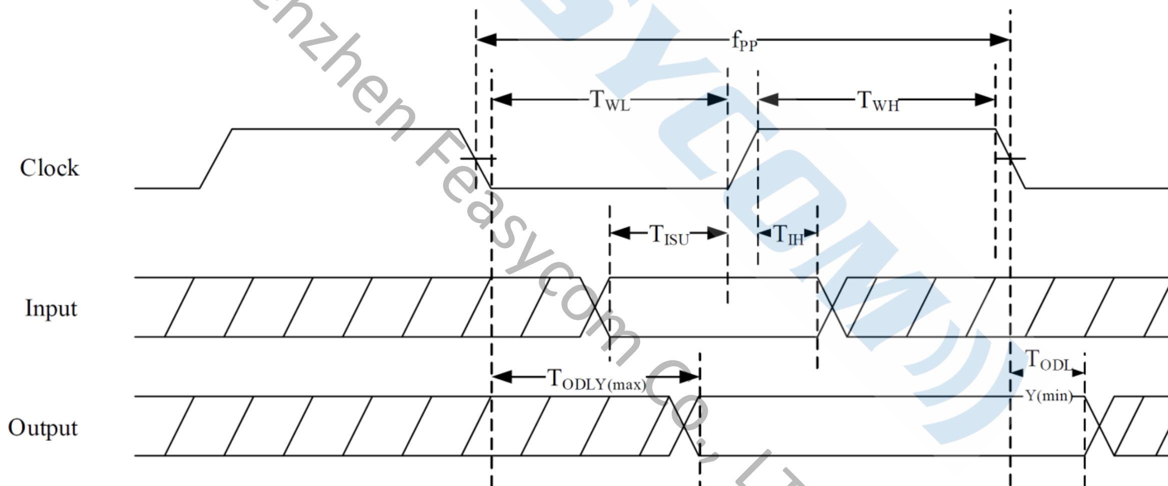

Figure 5-1-2-1: SDIO Interface Timing (default speed)

Table 5-1-2-1: SDIO Interface Timing Parameters (default speed)

Symbol	Parameter	Min.	Max.	Unit
f_{PP}	Clock Frequency	0	25	MHz
T_{WL}	Clock Low Time	10	-	ns
T_{WH}	Clock High Time	10	-	ns
T_{ISU}	Input Setup Time	5	-	ns
T_{IH}	Input Hold Time	5	-	ns
T_{ODLY}	Output Delay Time During Data Transfer Mode	0	14	ns
T_{ODLY}	Output Delay Time During Identification Mode	0	50	ns

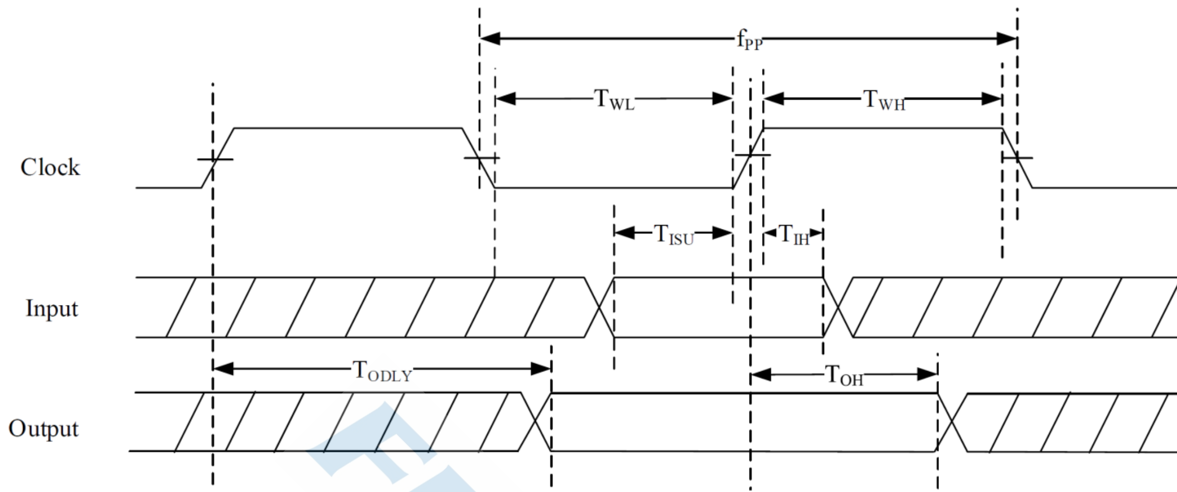

Figure 5-1-2-2: SDIO Interface Timing (high speed)

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Table 5-2-2-2: SDIO Interface Timing Parameters (high speed)

Symbol	Parameter	Min.	Max.	Unit
f_{PP}	Clock Frequency	0	50	MHz
T_{WL}	Clock Low Time	7	-	ns
T_{WH}	Clock High Time	7	-	ns
T_{ISU}	Input Setup Time	6	-	ns
T_{IH}	Input Hold Time	2	-	ns
T_{ODLY}	Output Delay Time During Data Transfer Mode	-	14	ns
T_{ODLY}	Output Delay Time During Identification Mode	2.5	-	ns

5.1.3 SDIO Interface Power-on Sequence

After power-on, the SDIO interface is selected by the module automatically when a valid SDIO command is received. To attain better SDIO host compatibility, the following power-on sequence is recommended.

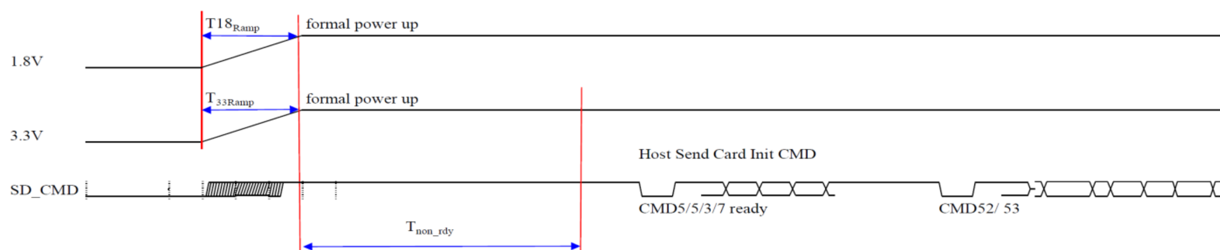

Figure 5-1-3-1: SDIO Interface Power-On Sequence

Table 5-1-3-1: SDIO Interface Power-On Sequence

Symbol	Description
T_{18_Ramp}	The 1.8V power ramp up duration.
T_{33_Ramp}	The 3.3V power ramp up duration.
T_{non_rdy}	SDIO Not Ready Duration. In this state, the RTL8733BS may respond to commands without the ready bit being set. After the ready bit is set, the host will initiate complete card detection procedure.

We recommend that the card detection procedures are divided into two phases: A 3.3V power pre-charge phase and a formal power-up phase.
After main 3.3V ramp up and 1.8V ramp up, the power management unit is enabled by the power ready detection circuit. The power management unit enables the SDIO block. eFUSE is then autoloaded to SDIO circuits during the Tnon_rdy duration. After CMD5/5/3/7 procedures, card detection is executed. When the driver has loaded, normal CMD52 and CMD53 are used.

Table 5-1-3-2: SDIO Interface Power-On Timing Parameters

Symbol	Min.	Typ.	Max.	Unit
T_{18_Ramp}	0.2	0.5	2.5	ms
T_{33_Ramp}	0.2	0.5	2.5	ms
T_{non_rdy}	1	2	10	ms

5.2 UART Interface Characteristics

The FSC-BW2231 UART interface is a 3-wire interface with RX, TX, CTS. The interface supports the Bluetooth 2.0 UART HCI H4 and H5 specifications. The default baud rate is 115.2 k baud. In order to support high and low speed baud rate, the FSC-BW2231 provides multiple UART clocks.

Baud Rate error rate: Per byte (including start/stop bit) +/- 1.3%

The UART signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the module UART interface via the VDDIO pin.

5.2.1 UART Interface Timing

The interface includes four signals, TXD/RXD/CTS/RTS. Flow control between the host and the device is byte-wise by hardware. When the HCI_CTS signal is set high, the device stops transmitting on the interface.
If HCI_CTS is set high in the middle of transmitting a byte, the device finishes transmitting the byte and stops the transmission.

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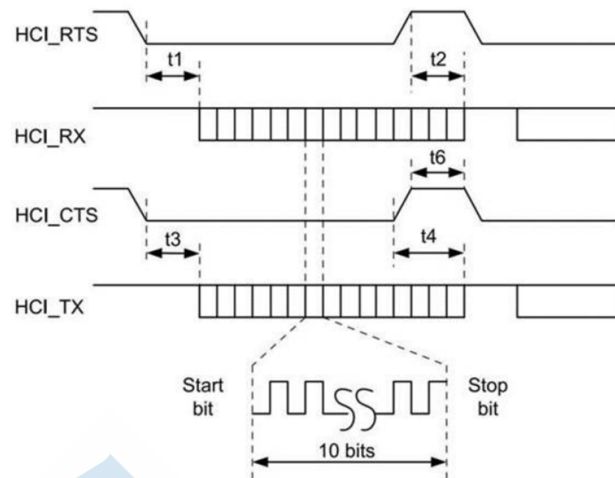

Figure 5-2-1-1: UART Timing Diagram

Table 5-2-1-1： UART Timing Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
	Baud rate		115.2		3000	Kbps
	Baud rate accuracy per	Receive/Transmit	-3		3	%
T3	CTS low to TX_DATA on		0	2		ns
T4	CTS high to TX_DATA off	Hardware flow			1	byte
T6	CTS High Pulse Width		1			bit
T1	RTS low to RX DATA on		0	2		ns
T2	RST high to RX_DATA off				1	HCI packet*

Note: HCI packet means HCI command (256 bytes), HCI event (256 bytes), ACL (1024 bytes), SCO (256 bytes).

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5.3 PCM Interface Characteristics

The RTL8733 supports a PCM digital audio interface that is used for transmitting digital audio/voice data to/from the Audio Codec. Features are supported as below:

- Supports Master and Slave mode
- Programmable long/short Frame Sync
- Supports 8-bit/16-bit linear PCM formats
- PCM Master Clock Output: 64, 128, 256, or 512kHz
- Supports SCO/ESCO link

5.3.1 PCM Format

FrameSync is the synchronizing function used to control the transfer of DAC_Data and ADC_Data. A Long FrameSync indicates the start of ADC_Data at the rising edge of FrameSync (see Figure 5-2-1), and a Short FrameSync indicates the start of ADC_Data at the falling edge of FrameSync (see Figure 5-2-2).

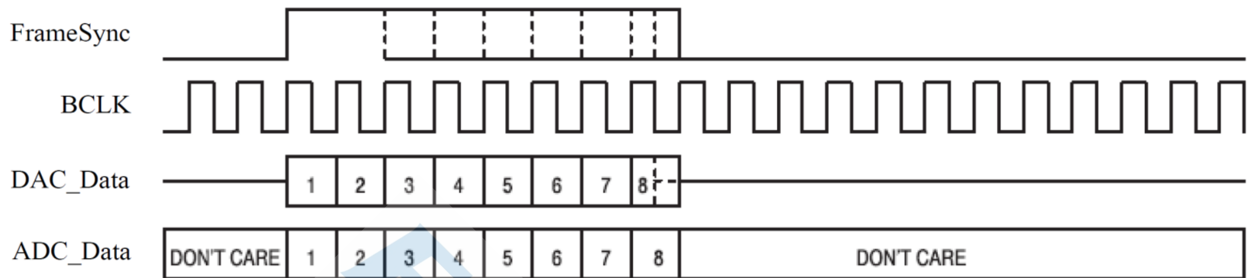

Figure 5-3-1-1: Long FrameSync

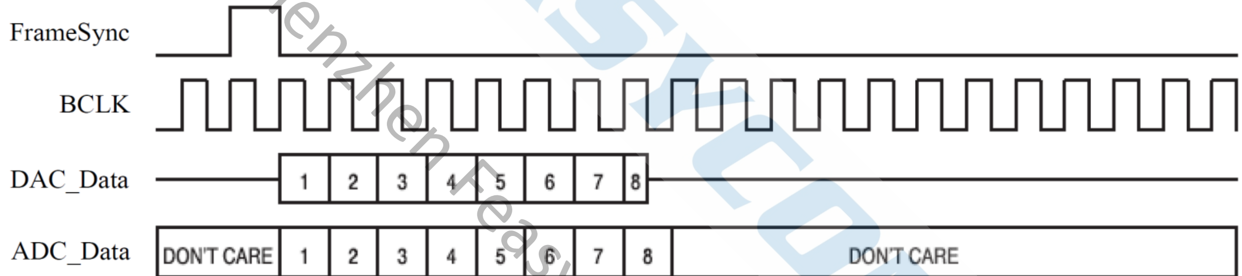

Figure 5-3-1-2: Short FrameSync

5.4 Power off by WL_DIS# and BT_DIS# sequence

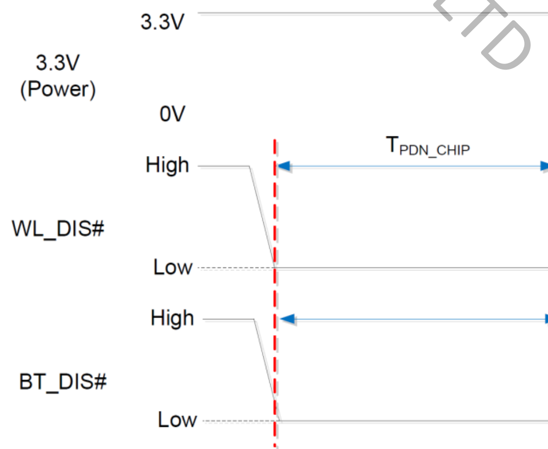

Figure 5-4-1: Power Off by WL# and BT_DIS# Sequence

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Table 5-4-1: Power Off by WL# and BT_DIS# Timing Parameters

Symbol	Min.	Typ.	Max.	Unit	Description
T_{PDN_CHIP}	10	100	-	ms	WL_DIS#, BT_DIS# keep low duration

5.5 Power off by 3.3V supply power sequence

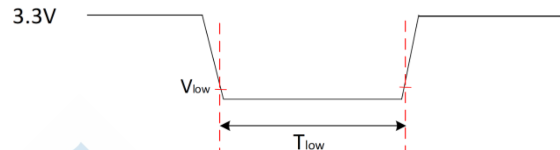

Figure 5-5-1: Power Off by WL# and BT_DIS# Sequence

Table 5-5-1: Power Off by 3.3V supply power Timing Parameters

Symbol	Description	Min.	Typ.	Max.	Unit
T_{low}	Supply power keep low duration	10	100	-	ms
V_{low}	Low power threshold	-	-	0.4	V

FSC-BW2231 can be powered off by cutting off the 3.3V power supply. The keeping low duration must be more than T_{low} and the voltage must be less than V_{low}.

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6 MSL & ESD

Table 6-1: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade	Electrostatic discharge
ESD – ESD_HAND_HBM -Human body model contact discharge per JEDEC EID/JESD22-A114F-2008	Pass ±3500V, all pins
ESD – ESD_HAND_CDM -Charged device model contact discharge per JEDEC EIA/JESD22-C101F-2013	Pass ±500 V, all pins

7 RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below , the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Notice (注意) :

Feasycom module must use Step-Stencil, suggestion using the stencil thickness about 0.16-0.2mm,it could be modify with the product.

使用我司模块，须使用阶梯钢网，建议阶梯钢网厚度0.16-0.20mm，可根据自己产品适应性，进行相应调整.

Table 7-1: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

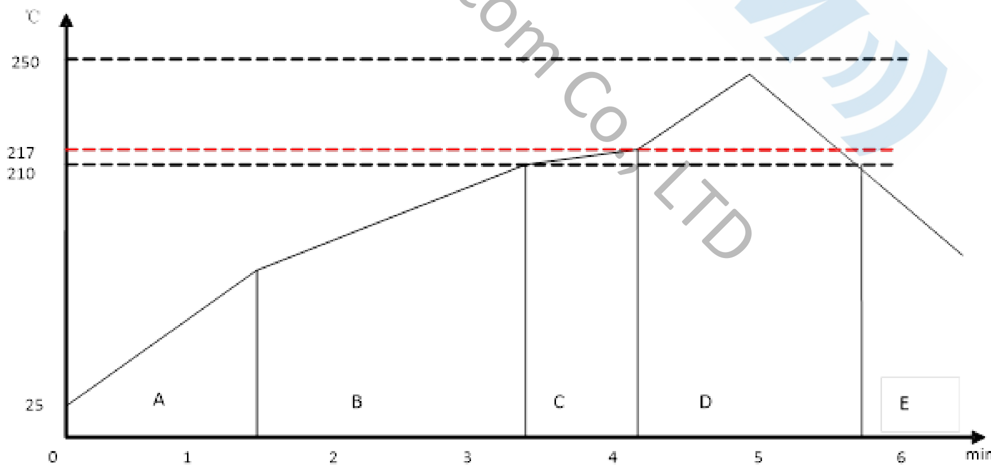

Figure 7-1: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and

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liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8 MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 12mm(W) x 12mm(L) x 2.2mm(H) Tolerance: ±0.2mm
- Module size: 12mm x 12mm Tolerance: ±0.2mm
- Pad size: 1.7mm x 0.5mm Tolerance: ±0.1mm
- Pad pitch: 0.9mm Tolerance: ±0.1mm

(分板后边角残留板边误差：不大于 0.5mm) (Residual plate edge error: < 0.5mm)

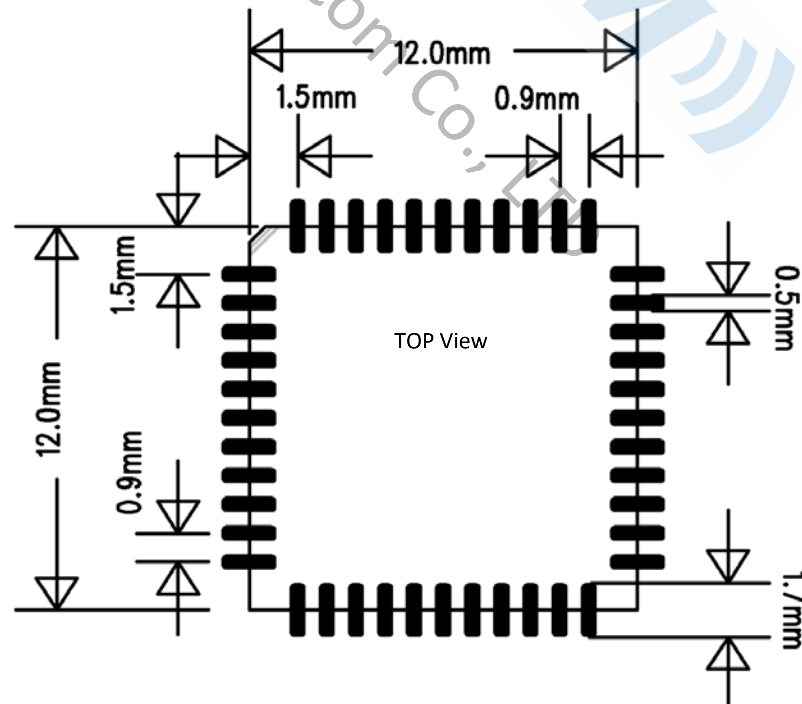

Figure 8-1-1：FSC-BW2231 footprint Layout Guide (Top View)

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9 HARDWARE INTEGRATION SUGGESTIONS

9.1 Requirement for the 3.3V power supply

- To use a dedicated power supply circuit for Wi-Fi (and BT).
- <0.05% line regulation and <0.5%/A load regulation are required for ripple frequency below 100KHz.
- Transient-response: 1, The ripple raised from 100/800mA step-response test should be small than 200mVpp.
  2, The ripple swing shall settle down within 1~2 cycles, 2 cycles for the worst case.
- Power supply spur: make sure the spurs from switching mode power supply or other noisy circuits are reasonably small. Once issue concerned with such a power supply spur, alternative power supply filtering might be needed.
- VDD_3V3: 3.15 to 3.45V (Peak Current 300mA); VDD_IO: 1.7 to 3.45V (Peak Current 100mA)

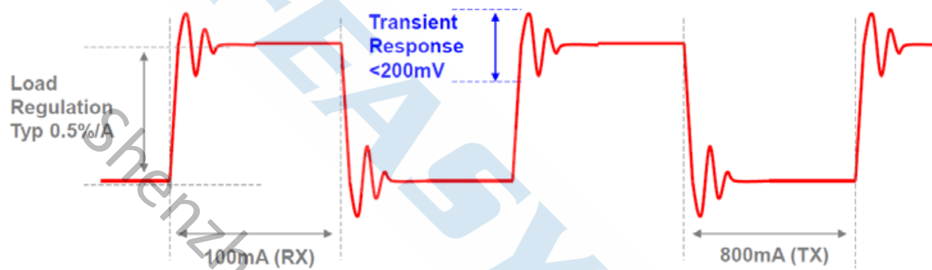

Figure 9-1-1: Requirement for the 3.3V power supply

9.2 RF Circuit- RF pads

- Some RF components such as 0402-packaged RLC, connectors, or module pins are with large soldering pad, those pads have higher parasitic capacitance which can impact the characteristic impedance of RF traces.
- The GND under those pads shall be dug out, shown as below, for keeping good 50Ω matching.
- The dig-out layers and area should be calculated carefully, we recommend digging the area a little higher than the simulation results.

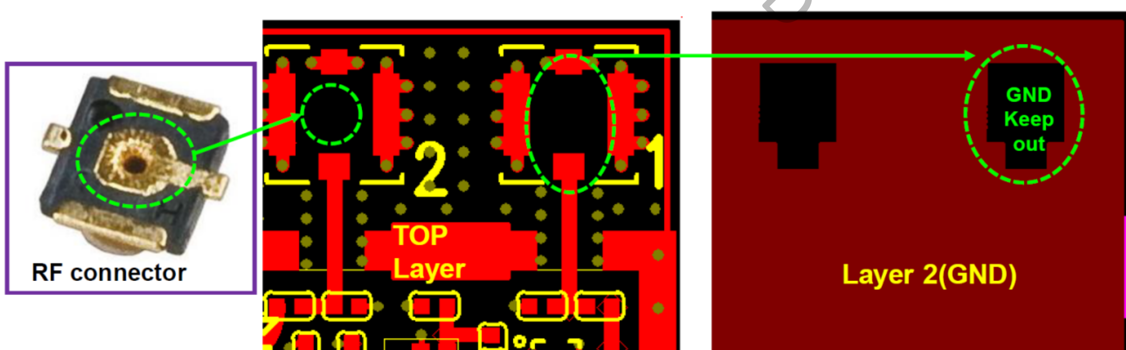

Figure 9-2-1: RF Circuit- RF pads

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9.3 Recommendable antenna & IPEX by Feasycom

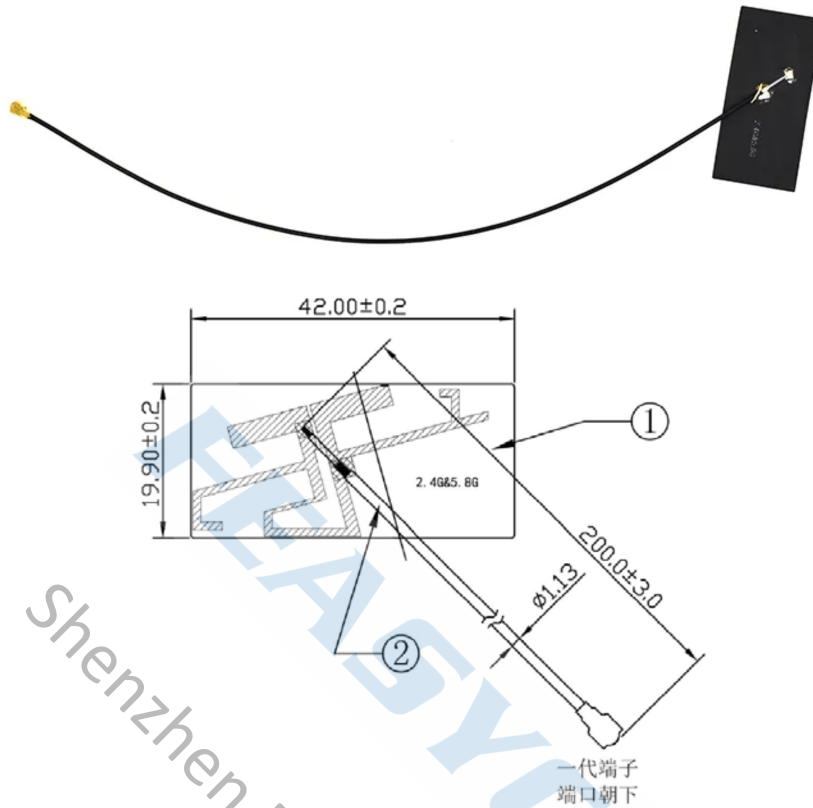

Figure 9-3-1: 2.4GHz & 5GHz Dual-band antenna, with IPEX first generation interface

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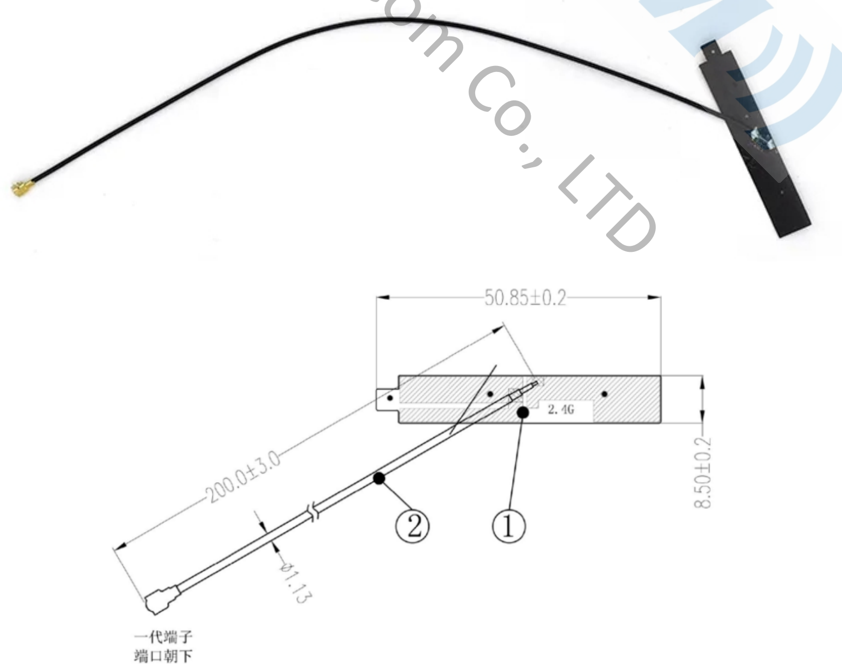
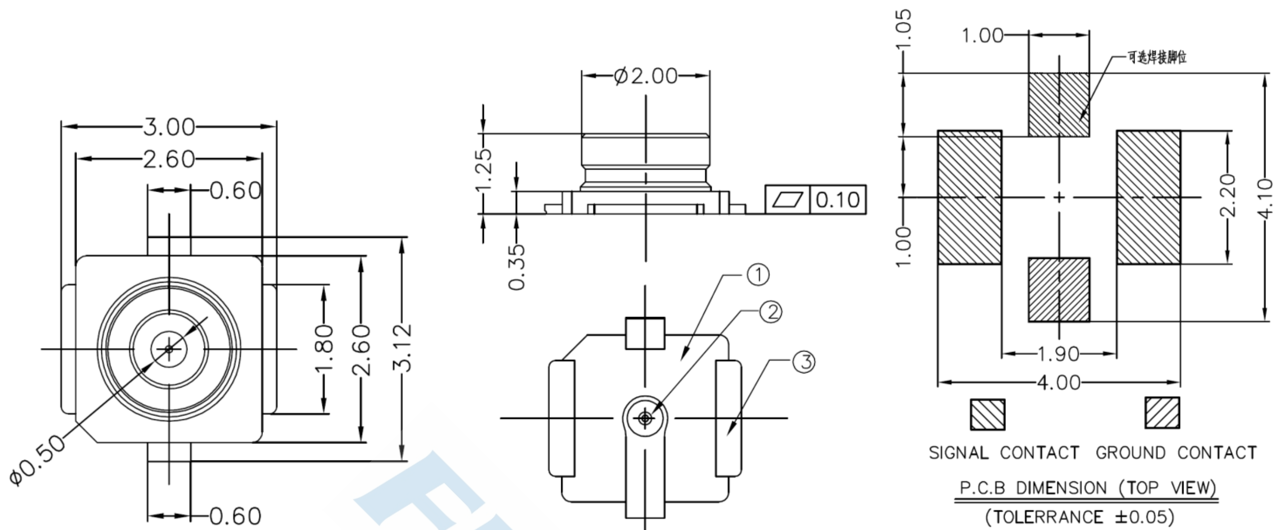


Figure 9-3-2: 2.4GHz antenna with IPEX first generation interface



3	GROUND CONTACT	1	JIS C5191-H	Au 1u" Min. over Ni 50~100u" Min.
2	CONTACT	1	JIS C2680-1/4H	Au 1u" Min. over Ni 50~100u" Min.
1	HOUSING	1	LCP E6808	UL94V-0,30% GF
ITEM	NAME	Q'TY	MATERIAL ⚠	FINISH ⚠

NOTES:
1. FREQUENCY RANGE:
   DC TO 6GHZ (VSWR: 1.3MAX AT 0.1~3GHZ, 1.4MAX AT 3~6GHZ)
2. CHARACTERISTIC IMPEDANCE: 50 (NOMINAL);
3. TEMPERATURE: −40°C TO +90°C;
4. RATED VOLTAGE : 60VAC;
5. CONTACT RESISTANCE :
   20m MAX.(SIGNAL CONTACT)
   20m MAX.(GROUND CONTACT)
6. WITHSTAND VOLTAGE : 200VAC FOR 1 MINUTE MIN;
7. INSULATION RESISTANCE : 500M MIN. AT 100VDC;
8. THIS COMPONENT IS HALOGEN FREE.

Figure 9-3-3: IPEX first generation interface

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9.4 Soldering Recommendations

FSC-BW2234 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.5 Layout Guidelines (Internal Antenna)

Important Note: The antenna for FSC-BW2231 is suggested to support both 2.4GHz and 5.8GHz dual frequency bands. We recommend using external FPC dual-band antennas instead of PCB onboard antennas. The following are general instructions for PCB onboard antennas for reference only.

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

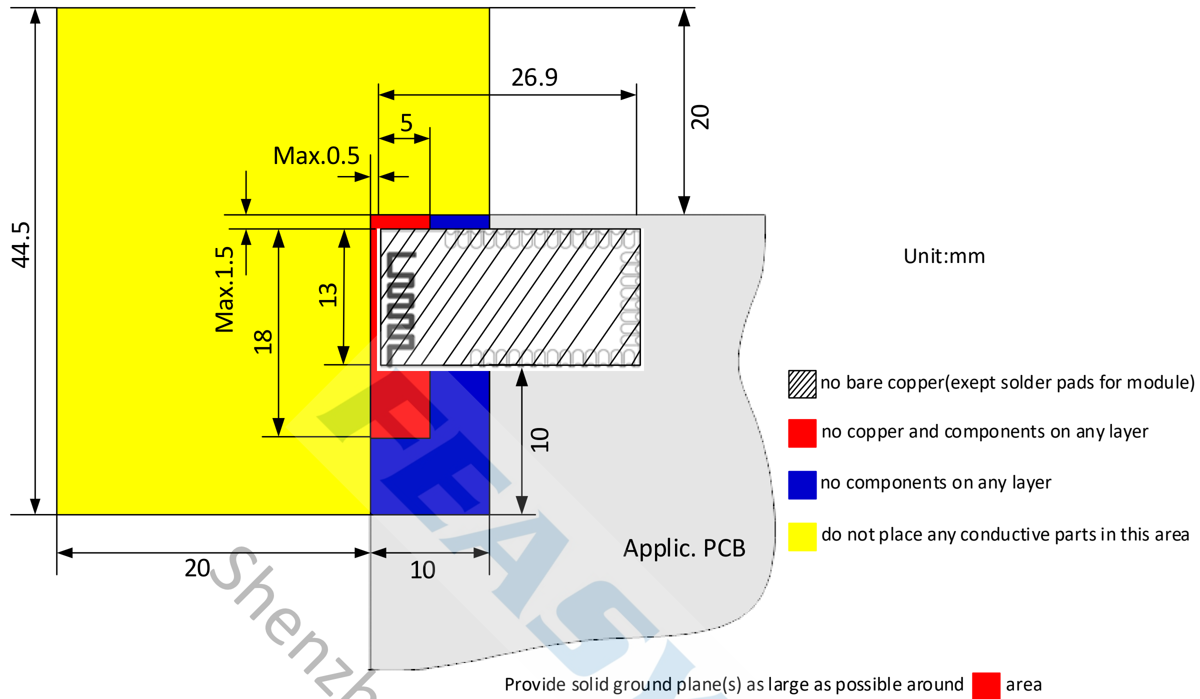

Figure 9-5-1: Restricted Area (Design schematic, for reference only. Unit: mm)

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

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9.6 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

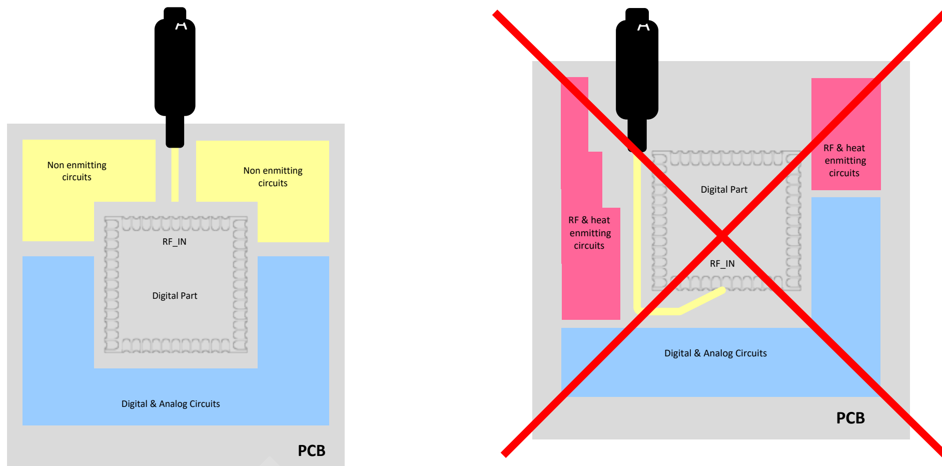

Figure 9-6-1: Placement the Module on a System Board

9.6.1 Antenna Connection and Grounding Plane Design

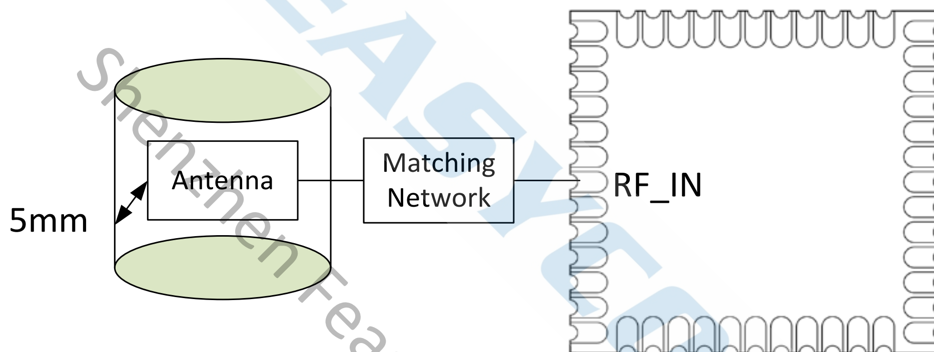

Figure 9-6-1-1: Leave 5mm Clearance Space from the Antenna

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General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

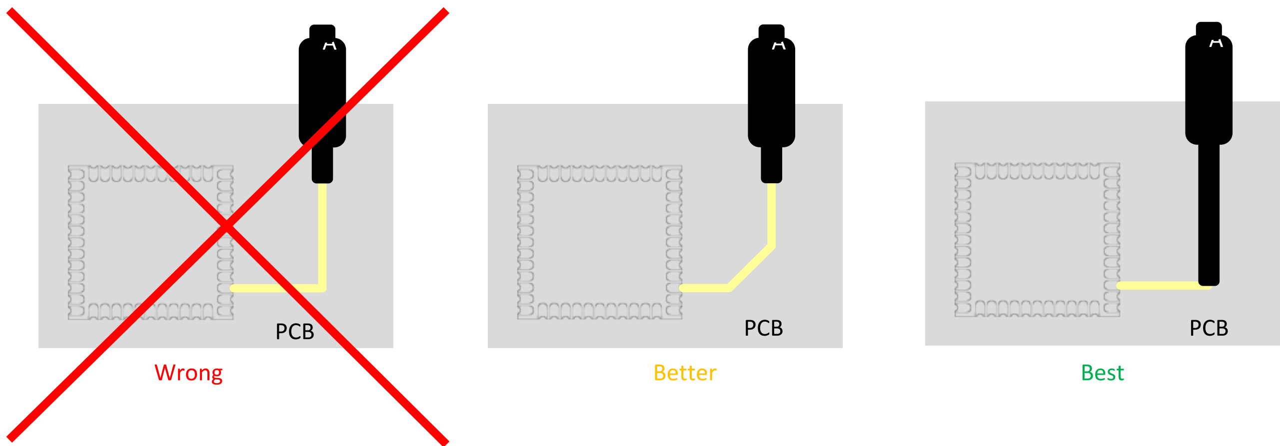

Figure 9-6-1-2: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

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9.7 SDIO Lines Layout Guideline

The following SDIO line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 8mA.

SDIO_CMD

SDIO_CLK

SDIO_D0 ~ SDIO_D3

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω

9.8 HCI Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 ~ 8mA

UART_RX

UART_TX

UART_CTS

UART_RTS

The route length of these signals be less than 15cm and the line impedance be less than 50Ω

9.9 Power Trace Lines Layout Guideline

VDD_3V3 Trace Width: 40mil

VDD_IO Trace Width: 20mil

9.10 Ground Lines Layout Guideline

A Complete Ground in Ground Layer.

Add Ground Through Holes to FSC-BW2231 Module Ground Pads

Decoupling Capacitors close to FSC-BW3321 Module Power and Ground Pads

10 PRODUCT PACKAGING INFORMATION

10.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 150mm * 150mm

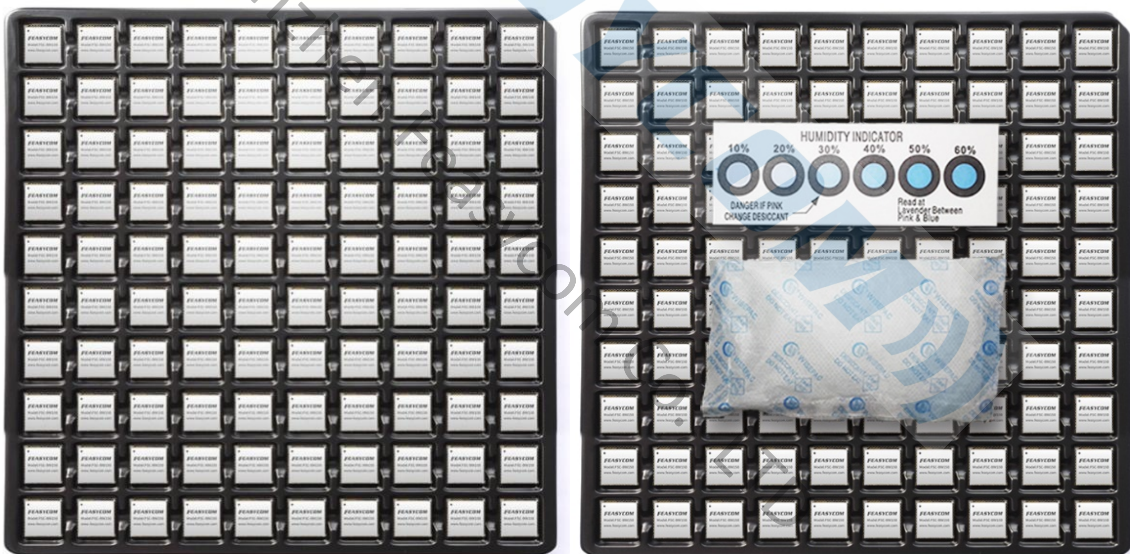

Figure 10-1-1: Tray vacuum

10.2 Packing box (Optional)

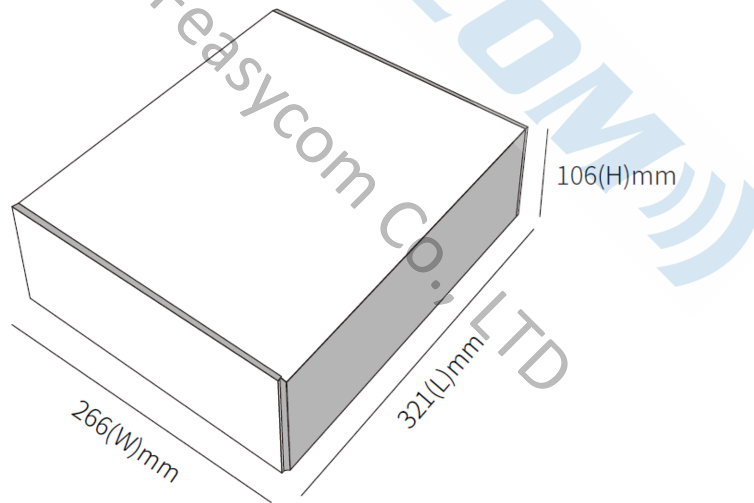

Figure 10-2-1: Packing box(Optional)

** If other packing is required, please confirm with the customer*

** Packing: 1000pcs per carton (Minimum packing quantity)*

** The outer packing size is for reference only, please refer to the actual size*

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11 APPLICATION SCHEMATIC

It is recommended to use the IPEX generation antenna base
and use the FPC dual frequency and single frequency antennas that have been verified by Feasycom.
The positions of the two antennas should be arranged at 90 degrees and at the farthest distance.

建议使用IPEX 一代天线座子，
并使用飞易通已经验证通过的FPC双频和单频天线
两条天线的位置呈90度摆放，并且呈最远距离摆放

Dual-band antenna:
2402MHz~2484MHz /4900MHZ~5925MHz

预留π型匹配电路
RF通路按50欧姆阻抗控制
Reserved π-type matching circuit RF path controlled by 50 ohm impedance

USRT Interface
UART1_CTS
UART_RX
UART1_TX
UART1_RTS

Reserved
预留上拉电阻，驱动能力弱时需要
Reserve pull-up resistor, which is required when the driving ability is weak.

BT_EN
POWER ON=1
POWER OFF=0

3.3V
3.0V~3.6V
3.3V需建议保证不小于1A的供电电流
VBAT主供电PCB走线宽度不小于1mm,
VIO供电PCB走线宽度不小于0.5mm,
模块底部不走任何线，并且大量的打接地孔
3.3V should ensure a power supply current of no less than 1A.

There should be no wires running at the bottom of the module,
and a large number of grounding holes should be drilled.

POWER ON=1
POWER OFF=0
WL_EN
SDIO_DATA2
SDIO_DATA3_WL
SDIO_DATA_CMD_WL
SDIO_DATA_CLK_WL
SDIO_DATA0_WL
SDIO_DATA1

SDIO通讯线要等长，CLK线要立体包地！
When designing a PCB, the SDIO CLK line needs to be solidly grounded.
SDIO communication lines need to be of equal length and have the shortest distance

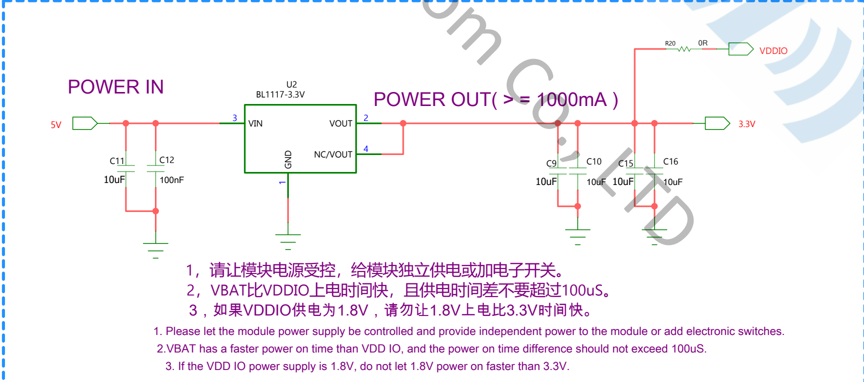
Reserved

PCM_SYNC
PCM_IN
PCM_CLK
PCM_OUT
PCM Interface

32.768KHz Input
Reserved
建议预留此电路，低功耗模式下的时钟源。
Optional. By default, this part of the circuit drawing is not used.

SUPPORT 1.62V~3.6V

预留位置，整机调试时再决定是否贴件。
电容靠近模块焊盘摆放。
（当主板电路复杂，PCB板线路较长，干扰较多时，建议加上此电容！）
Reserve a position and decide whether to place the capacitor near the module pad during the debugging of the entire machine.
(When the motherboard circuit is complex, the PCB circuit is long, and there is a lot of interference, it is recommended to add this capacitor)



1，请让模块电源受控，给模块独立供电或加电子开关。
2，VBAT比VDDIO上电时间快，且供电时间差不要超过100uS。
3，如果VDDIO供电为1.8V，请勿让1.8V上电比3.3V时间快。

1. Please let the module power supply be controlled and provide independent power to the module or add electronic switches.
2.VBAT has a faster power on time than VDD IO, and the power on time difference should not exceed 100uS.
3. If the VDD IO power supply is 1.8V, do not let 1.8V power on faster than 3.3V.

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