FSC-BT618V

Automotive qualified Bluetooth 5.2 low-energy wireless MCU

Module datasheet

Version 1.3

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Revision History

Version	Data	Notes	
1.0	2021/04/17	Initial Version	Fish
1.1	2021/04/29	Update block diagram	Fish
1.2	2021/11/04	Modify Bluetooth Version: Upgrade from BT5.1 to BT5.2 Change storage temperature：-40°C to +125°C	Marsh
1.3	2022/03/24	Update module pictures	Devin Wan

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1. INTRODUCTION

Overview

The FSC-BT618V is an AEC-Q100 compliant wireless microcontroller (MCU) targeting Bluetooth 5.2 Low Energy automotive applications. The device is optimized for low-power wireless communication in applications such as car access including passive entry passive start (PEPS) and remote keyless entry (RKE), battery management systems (BMS), car sharing, piloted parking, cable replacement, and smartphone connectivity. The highlighted features of this device include:

- Support Bluetooth 5.2 function: LE encoding PHY (long distance), LE 2-Mbit PHY (high speed),Ad expansion, multiple ad sets, CSA#2, and backward compatibility and support Main functions applicable to Bluetooth 5.2 and earlier low energy consumption specifications.Standard Bluetooth 5.2 software protocol stack software, can enable the angle of arrival (AoA).
- Longer battery life for wireless applications, with a low standby current of 0.94μA.
- AEC-Q100 conforms to the 2nd temperature range (-40°C to +105°C).
- Bluetooth low energy has excellent radio sensitivity and robustness (selectivity and blocking) performance (-105 dBm for 125 kbps LE coded PHY).

It supports GAP, ATT/GATT, SMP, L2CAP profile. It integrates the baseband controller in a small package (integrated chip antenna), so designers can provide better flexibility for product shape.

Features

- 2.4-GHz RF Transceiver Compatible With Bluetooth 5.2 Low Energy and earlier LE Specifications
- Excellent receiver sensitivity:
  – 105 dBm for Bluetooth 125-kbps (LE coded PHY)
  – 97 dBm for 1-Mbps PHY
- Qualified for automotive applicationsg
- AEC-Q100 qualified with the following results:
  – Device temperature grade 2: -40℃ to +105℃ ambient operating temperature range
  – Device HBM ESD Classification Level 2
  – Device CDM ESD Classification Level C3
- Integrate MCU to execute Bluetooth protocol stack
- Postage stamp sized form factor,
- Low power
- Class 1.5 support(Output power up to +5 dBm)
- The default UART Baud rate is 115.2Kbps and can support from 1200bps to 921.6Kbps
- UART, I2C,SPI,12-bit ADC(200 Ks/s) peripheral interfaces
- Support the OTA upgrade
- Support GATT, ATT, GAP, LE HID, and other BLE protocols
- PWM
- Support eight capacitance sensor button
- Integrated temperature sensor

Application

- Home and Building Automation
  – Connected Appliances
  – Lighting
  – Locks
  – Gateways
  – Security Systems
- Industrial
  – Logistics
  – Production and Manufacturing Automation
  – Asset Tracking and Management
  – HMI and Remote Display
  – Access Control

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- Retail
  - – Beacons
  - – Advertising
  - – ESL and Price Tags
  - – Point of Sales and Payment Systems
- Health and Medical
  - – Thermometers
  - – SpO2
  - – Blood Glucose and Pressure Meters
  - – Weight Scales
  - – Hearing Aids
- Sports and Fitness
  - – Activity Monitors and Fitness Trackers
  - – Heart Rate Monitors
  - – Running and Biking Sensors
  - – Sports Watches
  - – Gym Equipment
  - – Team Sports Equipment
- HID
  - – Voice Remote Controls
  - – Gaming
  - – Keyboards and Mice
- Automotive
  - – Car access and security systems
    - Passive entry passive start (PEPS)
    - Phone as a key (PaaK)
    - Remote keyless entry (RKE)
  - – Battery management system (BMS)
  - – Advanced driver assistance systems (ADAS)

Module picture as below showing

Figure 1: FSC-BT618V Picture

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2. General Specification

Table 1: General Specifications

Categories	Features	Implementation
Wireless Specification	Chip	TI CC2642R-Q1
	Bluetooth Version	Bluetooth 5.2 Low Energy(BLE)
	Frequency	2.402 - 2.480 GHz
	Transmit Power	+5 dBm (Maximum)
	Receive Sensitivity	-97 dBm for 1-Mbps PHY
		-105 dBm for 125-kbps LE Coded PHY
	Raw Data Rate (Air)	2 Mbps
	Modulation	GFSK
Host Interface and Peripherals	UART Interface	TX, RX, CTS, RTS
		General Purpose I/O
		Default 115200,N,8,1
		Baudrate support from 1200 to 921600
		5, 6, 7, 8 data bit character
	GPIO	18(maximum – configurable) lines
	I2C Interface	1 (configurable from GPIO total). Up to 400 kbps
	SSI Interface	Up to 2 SSI interfaces with a frequency of up to 4 MHz
		Support both master and slave mode
		SPI, MICROWIRE, TI
	ADC Interface	Analog input voltage range: 0V ~ 3.8V
		Supports single 12-bit SAR ADC conversion
		8 channels (configured from GPIO total)
		Sample rate up to 200 ksps
	PWM_(Timer)	4 General-Purpose Timer Modules
		Either 4× 32 bit timers or 8× 16 bit timers, all running on up to 48 MHz
Profiles	Class Bluetooth	No Support
	Bluetooth Low Energy	GATT Client & Peripheral - Any Custom Services
		BT5.2 Specifications
		MFI Support
Maximum Connections	Classic Bluetooth	No Support
	Bluetooth Low Energy	1 Clients
FW upgrade		Over the Air
		Xds
Supply Voltage	Supply	1.8V ~ 3.6V
Power Consumption		Max Peak Current(TX Power @ +5dBm TX): 9.6mA
		Standby Current : 0.94uA
		Deep Sleep : 150nA
Physical	Dimensions	13mm X 26.9mm X 2.2mm; Pad Pitch 1.5mm
Environmental	Operating	-40°C to +105°C

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	Storage	-40°C to +125°C
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:	Human Body Model	All pins: ±2000V
	Charged device model	RF pins/ Non-RF pins: ±500V

3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

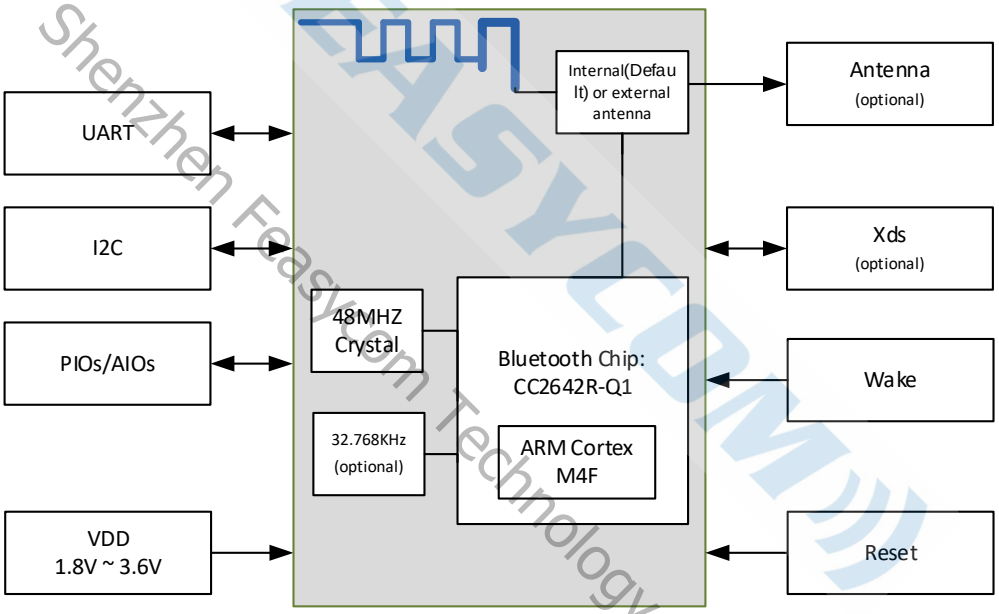

Figure 2: Block Diagram

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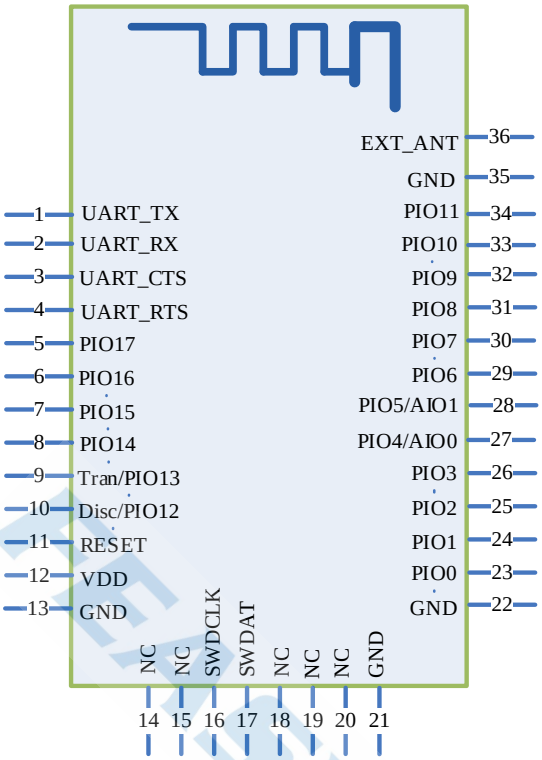

Figure 3: FSC-BT618V PIN Diagram(Top View)

3.2 PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	UART_TX	O	UART data output	Note 1
2	UART_RX	I	UART data input	Note 1
3	UART_CTS	I/O	UART clear to send active low Alternative Function: Programmable input/output line	Note 1
4	UART_RTS	I/O	UART request to send active low Alternative Function: Programmable input/output line	Note 1
5	PIO17	I/O	Programmable input/output line	
6	PIO16	I/O	Programmable input/output line	
7	PIO15	I/O	Programmable input/output line	
8	PIO14	I/O	Programmable input/output line	
9	Tran/PIO13	I/O	Programmable input/output line Alternative Function 1: Host MCU change UART transmission mode.	Note 1
10	Disc/PIO12	I/O	Programmable input/output line Alternative Function 2: Host MCU disconnect Bluetooth	Note 1
11	RESET	I	External reset input: Active LOW, with an inter an internal pull-up. Set this pin low to reset to initial state.	
12	VDD	Vdd	Power supply voltage 1.8V ~ 3.6V	
13	GND	Vss	Power Ground	

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14	NC		NC	
15	NC		NC	
16	SWDCLK	I/O	SWD CLK line(Default)	Note 1
17	SWDAT	I/O	SWD DATA line(Default)	Note 1
18	NC		NC	
19	NC		NC	
20	NC		NC	
21	GND	Vss	Power Ground	
22	GND	Vss	Power Ground	
23	**PIO0**	I/O	Programmable input/output line	
24	**PIO1**	I/O	Programmable input/output line	
25	**PIO2**	I/O	Programmable input/output line	
26	**PIO3**	I/O	Programmable input/output line	
27	PIO4/AIO0	I/O	Programmable input/output line Alternative Function 1: Analogue programmable I/O line.	
28	PIO5/AIO1	I	Programmable input/output line Alternative Function 1: Analogue programmable I/O line.	
29	PIO6	I/O	Programmable input/output line Alternative Function: I2C CLK line (Default)	Note 1,3
30	PIO7	I/O	Programmable input/output line Alternative Function: I2C DATA line (Default)	Note 1,3
31	PIO8	I/O	Programmable input/output line	
32	PIO9	I/O	Programmable input/output line Alternative Function: LED(Default)	Note 1,4
33	PIO10	I/O	Programmable input/output line Alternative Function: BT Status(Default)	Note 1,2
34	PIO11	I/O	Alternative Function: Programmable input/output line	Note 1
35	GND	Vss	RF Ground	
36	EXT_ANT	O	RF signal output .	Note 5

Module Pin Notes:

Note 1	For customized module, this pin can be work as I/O Interface.
Note 2	BT Status(Default)-- Disconnected: Low Level; Connected: High Level.
Note 3	I2C Serial Clock and Data. It is essential to remember that pull-up resistors on both SCL and SDA lines are not provided in the module and MUST be provided external to the module.
Note 4	LED(Default)-- Power On: Light Slow Shinning ; Connected: Steady Lighting.
Note 5	By default, this PIN is an empty feet. This PIN can connect to an external antenna to improve the Bluetooth signal coverage. If you need to use an external antenna, by modifying the module on the 0R resistance to block out the on-board antenna; Or contact Feasycom for modification.

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4. PHYSICAL INTERFACE

4.1 Power Supply

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less. It is essential that the power rail recovers quickly.

4.2 Reset

The module may be reset from several sources: Power-on Reset (POR), Low level on the nRESET Pin (nRST), Watchdog time-out reset (WDT), Low voltage reset (LVR) or Software Reset(SYSRESETREQ, CPU Reset, CHIPRST).

The RESET pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESET being active. It is recommended that RESET be applied for a period greater than 5ms.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The PIOs have weak pull-ups.

4.3 General Purpose Analog IO

- 12-bit SAR ADC engine with up to 200KSPS conversion rate
- Conversion range: VSSA to VDDA (0 to 3.6 V)
- Temperature sensor

Twelve 12-bit 1 μs multi-channel ADC is integrated in the device.

The conversion range is between 0 V < VDD < 3.6 V. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block of analog inputs also can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced usages. The ADC can be triggered from the events generated by the general-purpose timers and the advanced-control timers with internal connection.

The temperature sensor can be used to generate a voltage that varies linearly with temperature. Each device is factory-calibrated to improve the accuracy and the calibration data are stored in the system memory area.

4.4 General Purpose Digital IO

There are 18 general purpose digital IOs defined in the module. All these GPIOs can be configured by software to realize various functions, such as button controls, LED drives or interrupt signals to host controller, etc. Do not connect them if not use.

The I/O type of each I/O pins can be configured by software individually as Input or Push-pull output mode. After the chip is reset, the I/O mode of all pins is input mode with no pull-up and pull-down enable. Each I/O pin has an individual pull-up and pull-down resistor which is about 30 kΩ ~ 50 kΩ for VDD and Vss.

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4.5 RF Interface

For this module, it has an on-board antenna and the interface for external antenna. The external antenna can be applied, by modifying a 0ohm resistor to block out the on-board antenna; Or contact Feasycom for modification.

The user can connect a 50 ohm antenna directly to the RF port.

- 2402–2480 MHz Bluetooth 5.2; 125-Kbps to 2-Mbps over the air data rate.
- TX output power of +5dBm.
- Receiver to achieve maximum sensitivity -95dBm @ 1 Mbps BLE.

4.6 Serial Interfaces

4.6.1 UART

FSC-BT618V provides one channels of Universal Asynchronous Receiver/Transmitters(UART)(Full-duplex asynchronous communications). The UART Controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART Controller channel supports ten types of interrupts.

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

This module output is at 3.3V CMOS logic levels (tracks VCC). Level conversion must be added to interface with an RS-232 level compliant interface.

Some serial implementations link CTS and RTS to remove the need for handshaking. We do not recommend linking CTS and RTS except for testing and prototyping. If these pins are linked and the host sends data when the FSC-BT618V deasserts its RTS signal, there is significant risk that internal receive buffers will overflow, which could lead to an internal processor crash. This drops the connection and may require a power cycle to reset the module. We recommend that you adhere to the correct CTS/RTS handshaking protocol for proper operation.

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Table 3: Possible UART Settings

Parameter		Possible Values
Baudrate	Minimum	1200 baud (≤2%Error)
	Standard	115200bps(≤1%Error)
	Maximum	921600bps(≤1%Error)
Flow control		RTS/CTS, or None
Parity		None, Odd or Even
Number of stop bits		1 /1.5/2
Bits per channel		5/6/7/8

When connecting the module to a host, please make sure to follow .

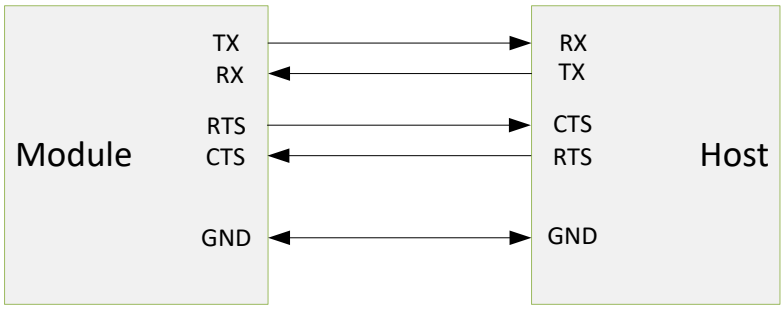

Figure 4: UART Connection

4.6.2 I²C Interface

- Up to two I²C bus interfaces can support both master and slave mode with a frequency up to 400KHZ.
- Provide arbitration function, optional PEC(packet error checking) generation and checking.
- Supports 7 –bit and 10 –bit addressing mode and general call addressing mode.

The I²C interface is an internal circuit allowing communication with an external I²C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I²C module provides two data transfer rates: 100 kHz of standard mode or 400kHz of the fast mode. The I²C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I²C bus at the same time. A CRC-8 calculator is also provided in I²C interface to perform packet error checking for I²C data.

4.7 SSI Interface

The SSIs are synchronous serial interfaces that are compatible with SPI, MICROWIRE, and Texas Instruments synchronous serial interfaces. The SSIs support both SPI master and slave up to 4 MHz.

4.8 PWM Interface

The four flexible GPTIMERs can be used as either 4× 32 bit timers or 8× 16 bit timers, all running on up to 48 MHz. Each of the 16- or 32-bit timers support a wide range of features such as one-shot or periodic counting, pulse width modulation (PWM), time counting between edges and edge counting. The inputs and outputs of the timer are connected to the device event fabric, which allows the timers to interact with signals such as GPIO inputs, other timers, DMA and ADC.

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below. Exceeding these values causes permanent damage.

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The average PIO pin output current is defined as the average current value flowing through any one of the corresponding pins for a 100mS period. The total average PIO pin output current is defined as the average current value flowing through all of the corresponding pins for a 100mS period. The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

Table 4: Absolute Maximum Rating

Parameter	Min	Max	Unit
V_{DD}-V_{SS} - DC Power Supply	-0.3	+4.1	V
V_{IN} - Voltage on any digital pin	-0.3	Vdd+0.3(max 4.1)	V
V_{IN} - Voltage on ADC input (Voltage scaling enabled)	-0.3	Vdd	V
V_{IN} - Voltage on ADC input (Voltage scaling disabled, VDDS as reference)	-0.3	VDD / 2.9	V
Input RF level		5	dBm
T_{ST} - Storage Temperature	-40	+125	°C
I_{IO} - Maximum Current sunk by a I/O pin		8	mA
I_{IO} - Maximum Current sourced by a I/O pin		8	mA

5.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
V_{DD}-V_{SS} - DC Power Supply	1.8	3.3	3.6	V
T_A - Operating Temperature	-40	25	+105	°C
I_{IO} - Maximum Current sunk by a I/O pin	2	4	6	mA
I_{IO} - Maximum Current sourced by a I/O pin	2	4	6	mA

5.3 Input/output Terminal Characteristics

Table 6: DC Characteristics

Parameter	Min	Type	Max	Unit
V_{DD} = 1.8V, T_A = 25°C				
V_{OH} - High Level Output Voltage, I_{IO}=8mA IOCURR = 2, high-drive GPIOs only	-	1.56	-	V
V_{OL} - Low Level Output Voltage, I_{IO}=8mA IOCURR = 2, high-drive GPIOs only	-	0.24	-	V
V_{OH} - High Level Output Voltage, I_{IO}=4mA , IOCURR = 1	-	1.59	-	V
V_{OL} - Low Level Output Voltage, I_{IO}=4mA , IOCURR = 1	-	0.21	-	V
GPIO pullup current - Input mode, pullup enabled, Vpad = 0 V	-	73	-	uA
GPIO pulldown current - Input mode, pulldown enabled, Vpad = VDD	-	19	-	uA
GPIO low-to-high input transition, with hysteresis - IH = 1, transition voltage for input read as 0 → 1	-	1.08	-	V
GPIO high-to-low input transition, with hysteresis -	-	0.73	-	V

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IH = 1, transition voltage for input read as 1 → 0				
GPIO input hysteresis - IH = 1, difference between 0 → 1 and 1 → 0 points	-	0.35	-	V
V_{DD} = 3.0V, T_A = 25°C				
VOH - High Level Output Voltage, IIO=8mA IOCURR = 2, high-drive GPIOs only	-	2.59	-	V
VOL - Low Level Output Voltage, IIO=8mA IOCURR = 2, high-drive GPIOs only	-	0.42	-	V
VOH - High Level Output Voltage, IIO=4mA , IOCURR = 1	-	2.63	-	V
VOL - Low Level Output Voltage, IIO=4mA , IOCURR = 1	-	0.40	-	V
V_{DD} = 3.6V, T_A = 25°C				
GPIO pullup current - Input mode, pullup enabled, Vpad = 0 V	-	282	-	uA
GPIO pulldown current - Input mode, pulldown enabled, Vpad = VDD	-	110	-	uA
GPIO low-to-high input transition, with hysteresis - IH = 1, transition voltage for input read as 0 → 1	-	1.97	-	V
GPIO high-to-low input transition, with hysteresis - IH = 1, transition voltage for input read as 1 → 0	-	1.55	-	V
GPIO input hysteresis - IH = 1, difference between 0 → 1 and 1 → 0 points	-	0.42	-	V
T_A = 25°C				
VIH - Lowest GPIO input voltage reliably interpreted as a High	-	-	0.8	VDD
VIL - Lowest GPIO input voltage reliably interpreted as a LOW	0.2	-	-	VDD

5.4 Analog Characteristics

Table 7: Specifications of 12-bit SARADC(voltage scaling enabled, unless otherwise noted.(1))

Parameter	Min	Type	Max	Unit
V_{DDA} - Operation Voltage	0	-	3.6	V
R_{ADC} - Resolution	-	-	12	bit
F_{SPS} - Sampling Rate	-	-	200	KSPS
Offset (Internal 4.3-V equivalent reference(2))	-	-0.24	-	LSB
Gain error (Internal 4.3-V equivalent reference(2))	-	7.14	-	LSB
DNL(3) Differential nonlinearity	-	>–1	-	LSB
INL(4) Integral nonlinearity	-	±4	-	LSB
ENOB - Effective number of bits				
Internal 4.3-V equivalent reference(2), 200ksps,9.6-kHz input tone	-	9.8	-	bits
Internal 4.3 V equivalent reference(2), 200 kSamples/s,9.6 kHz input tone, DC/DC enabled	-	9.8	-	bits
Internal 1.44-V reference, voltage scaling disabled,32 samples average,	-	11.1	-	bits

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200ksps, 300-Hz input tone				
THD - Total harmonic distortion				
Internal 4.3-V equivalent reference(2), 200 ksps,9.6-kHz input tone	-	-65	-	bits
VDD as reference, 200ksps, 9.6-kHz input tone	-	-70	-	bits
Internal reference, voltage scaling disabled,32 samples average, 200ksps, 300-Hz input tone	-	-72	-	bits
SINAD,SNDR - Signal-to-noise and distortion ratio				
Internal 4.3-V equivalent reference(2), 200ksps,9.6-kHz input tone	-	60	-	dB
VDD as reference, 200ksps, 9.6-kHz input tone	-	63	-	dB
Internal 1.44-V reference, voltage scaling disabled,32 samples average, 200ksps, 300-Hz input tone	-	68	-	dB
SFDR - Spurious-free dynamic range				
Internal 4.3-V equivalent reference(2), 200ksps,9.6-kHz input tone	-	70	-	dB
VDD as reference, 200ksps, 9.6-kHz input tone	-	73	-	dB
Internal 1.44-V reference, voltage scaling disabled,32 samples average, 200ksps, 300-Hz input tone	-	75	-	dB
Conversion time - Serial conversion, time-to-output, 24-MHz clock	-	50	-	Clock-cycles
Current consumption - Internal 4.3-V equivalent reference(2)	-	0.42	-	mA
Current consumption - VDD as reference	-	0.6	-	mA
Reference voltage - VDDS as reference (Also known as RELATIVE) (input voltage scaling enabled)	-	VDD	-	V
Input impedance - 200 ksps, voltage scaling enabled. Capacitive input, Input impedance depends on sampling frequency and sampling time	-	>1	-	MΩ

(1) Using IEEE Std 1241™-2010 for terminology and test methods.
(2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V.
(3) No missing codes. Positive DNL typically varies from +0.3 to +3.5, depending on device.
(4) For a typical example.

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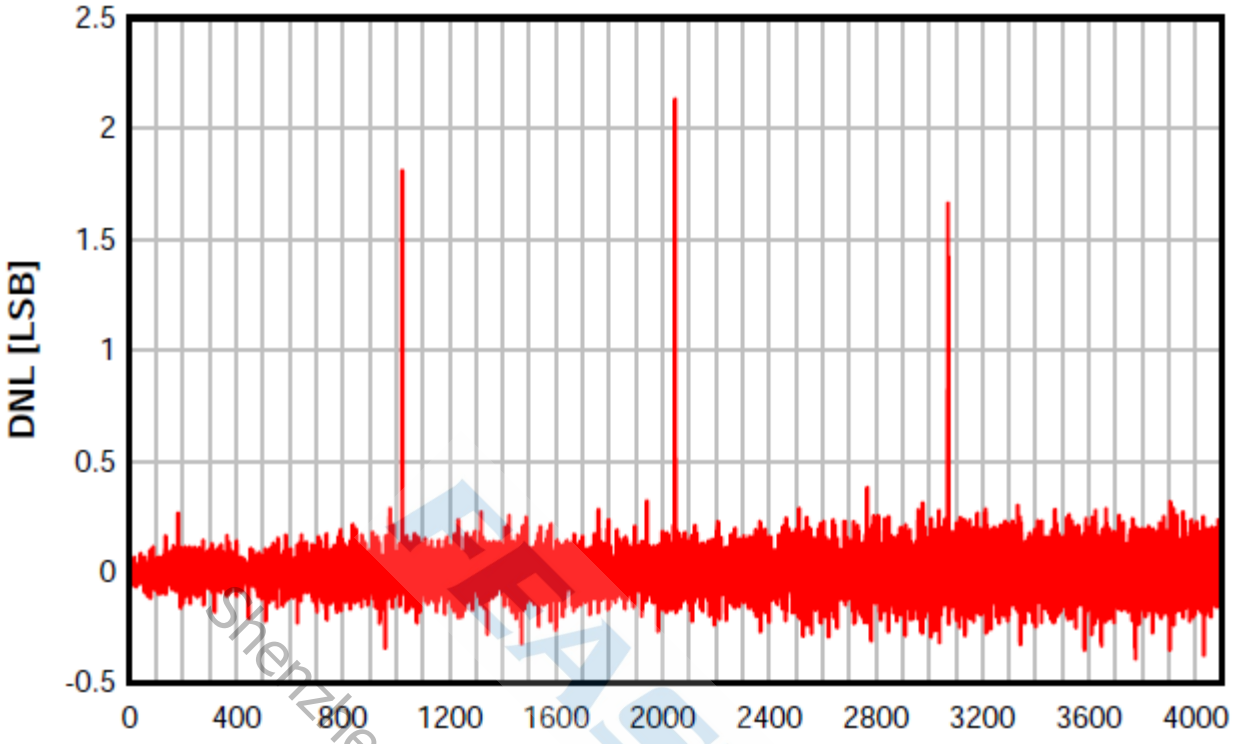

Figure 5: SoC ADC DNL vs ADC Code (Internal Reference)

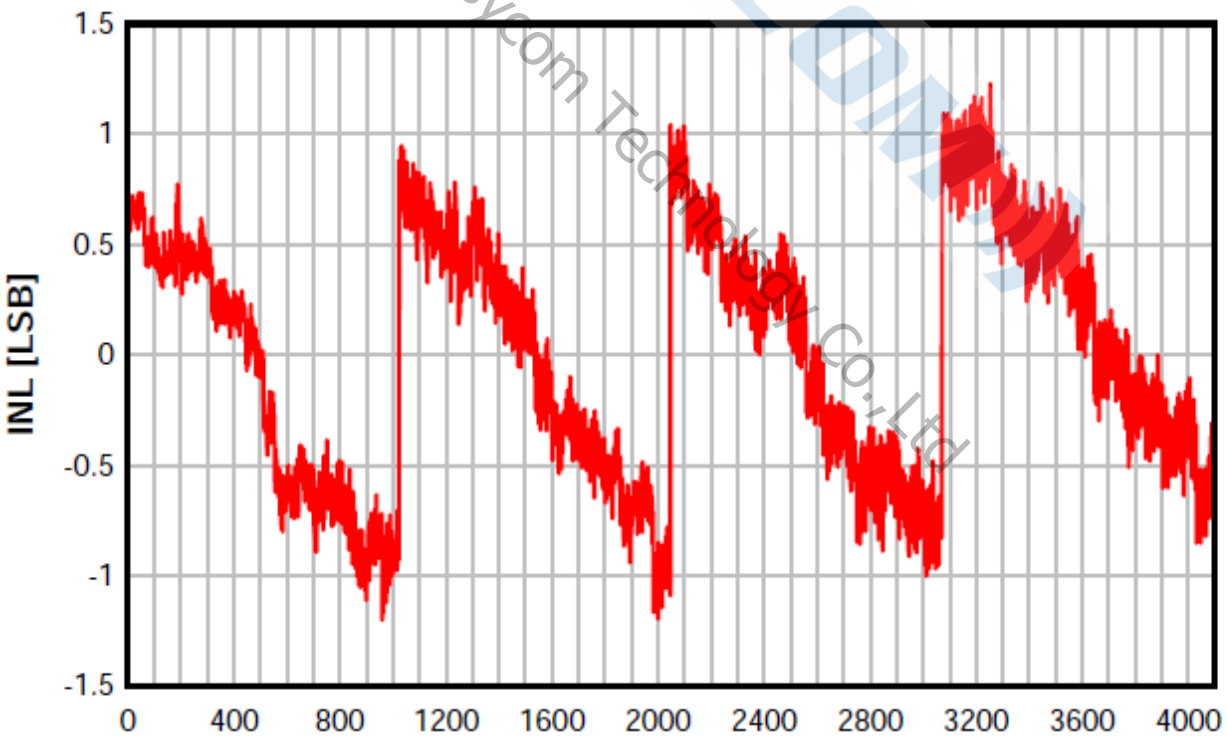

Figure 6: SoC ADC INL vs ADC Code (Internal Reference)

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5.5 Temperature Sensor

Table 8: Temperature Sensor (reference design with Tc = 25°C, VDD = 3.0 V, unless otherwise noted)

Parameter	Min	Type	Max	Unit
Resolution	-	2	-	°C
Accuracy (-40 °C to 0 °C)	-	±4.0	-	°C
Accuracy (0 °C to 85 °C)	-	±2.5	-	°C
Supply voltage coefficient(1)	-	3.6	-	°C /V

(1) Automatically compensated when using supplied driver libraries.

5.6 Battery Monitor

Table 9: Battery Monitor (reference design with Tc = 25°C, VDD = 3.0 V, unless otherwise noted)

Parameter	Min	Type	Max	Unit
Resolution	-	25	-	mV
Range	1.8	-	3.6	V
Accuracy	-	22.5	-	mV
Offset error		-32		mV

5.7 Synchronous Serial Interface (SSI)

Table 10: Synchronous Serial Interface (SSI) (Tc = 25°C, VDD = 3.0 V, unless otherwise noted.)

Parameter			Min	Type	Max	Unit
S1 t_{clk_per} (SSIClk period)	-	Device operating as SLAVE	12	-	65024	System clocks
S2 t_{clk_high} (SSIClk high time)	-	Device operating as SLAVE	-	0.5	-	t_{clk_per}
S3 t_{clk_low} (SSIClk low time)	-	Device operating as SLAVE	-	0.5	-	t_{clk_per}

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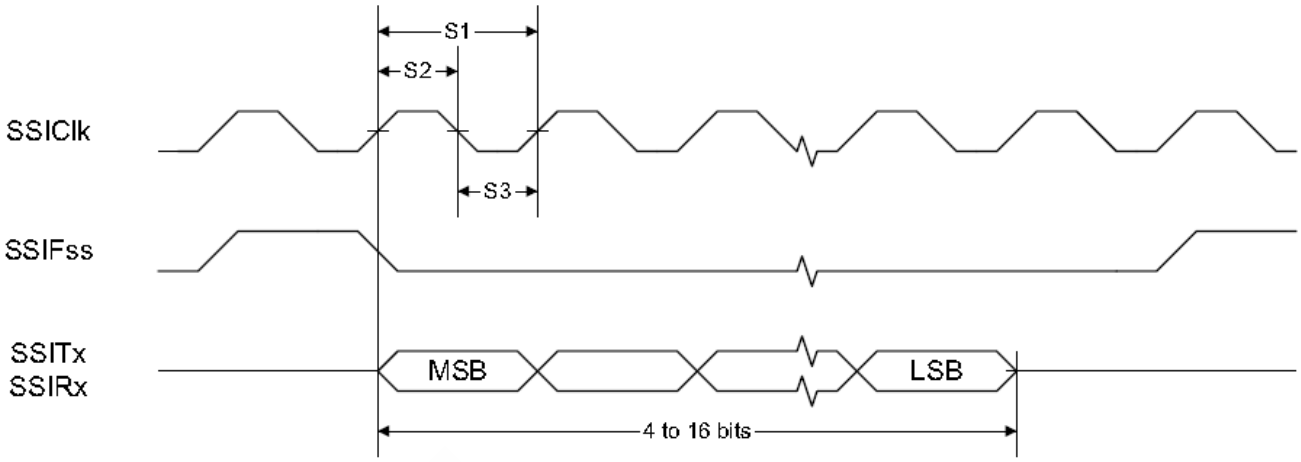

Figure 7: SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement

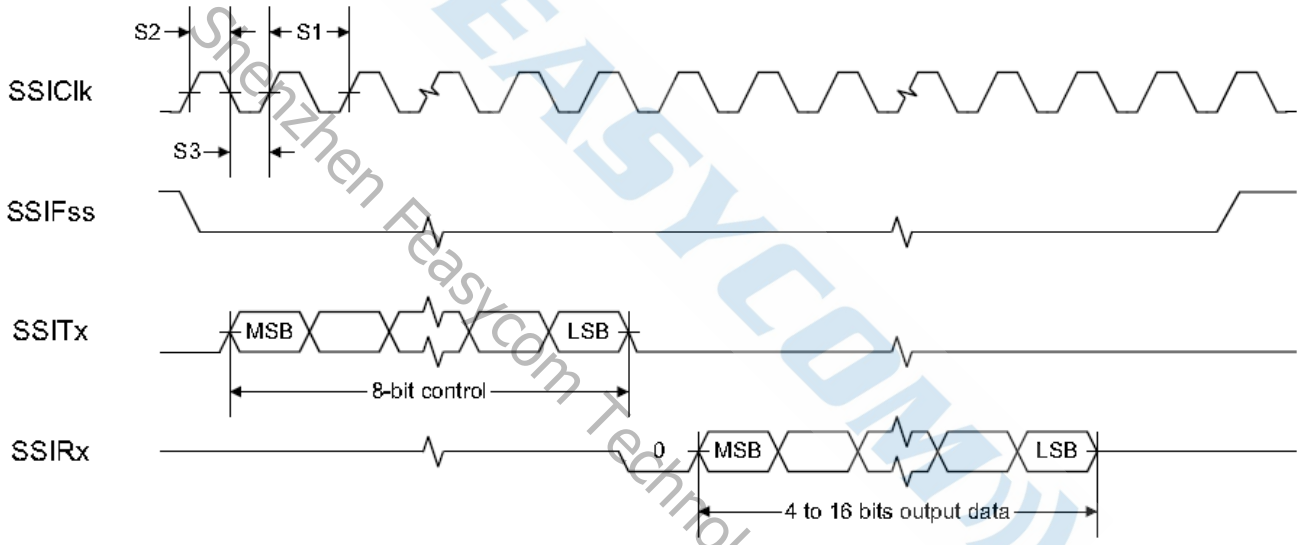

Figure 8: SSI Timing for MICROWIRE Frame Format (FRF = 10), Single Transfer

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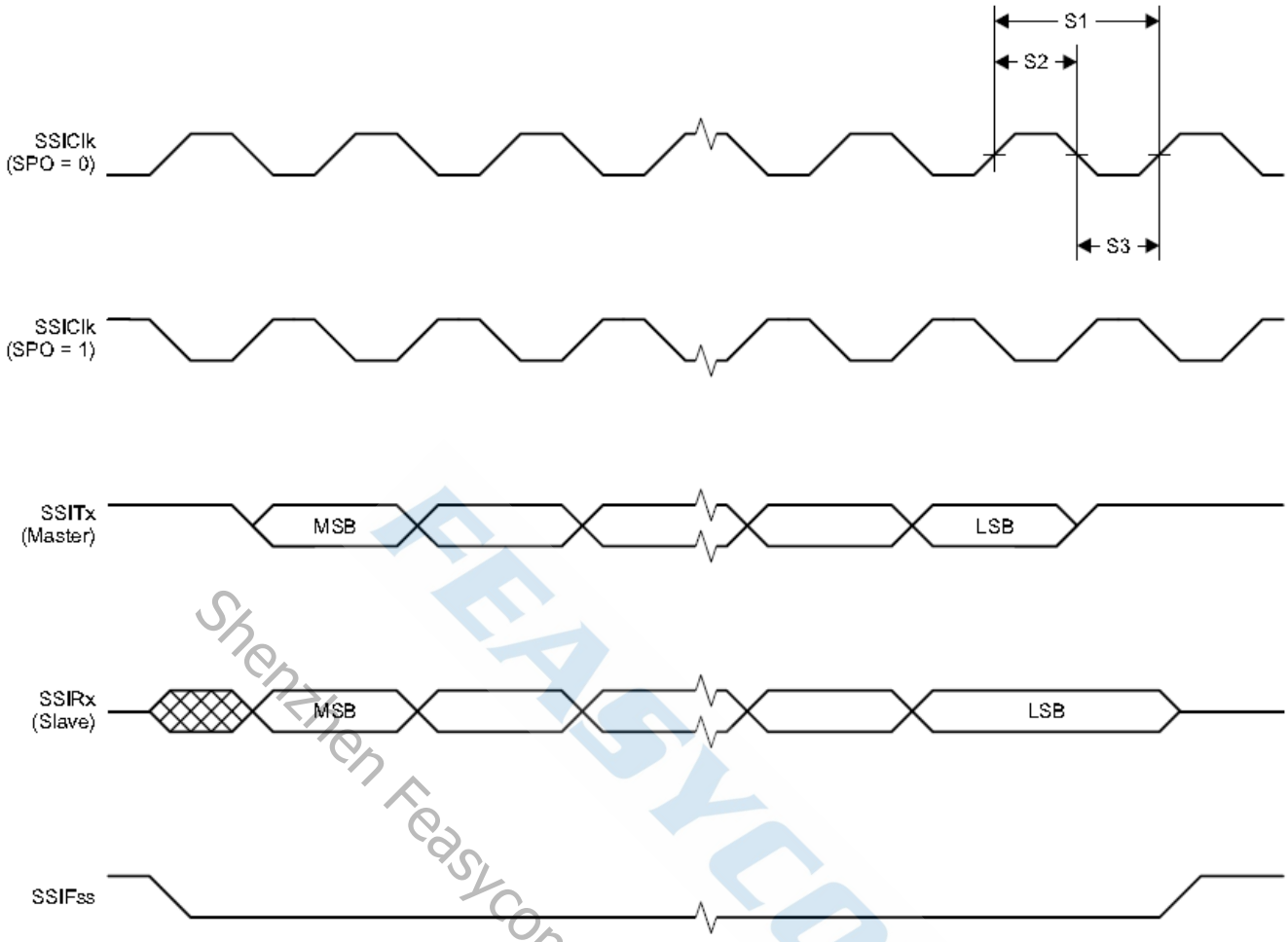

Figure 9: SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1

5.8 Switching Characteristics

Table 11: Switching Characteristics

Parameter	Min	Typ	Max	Unit
WAKEUP AND TIMING				
Idle → Active	-	14	-	uS
Standby → Active	-	160	-	uS
Shutdown → Active	-	850 - 3000-	-	uS

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5.9 Power consumptions

Table 12: Power consumptions

(When measured on the reference design with T_C = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted.)

Parameter	Test Conditions	Type	Unit
Radio receive current	2440MHz	6.9	mA
Radio transmit current	0 dBm output power setting 2440 MHz	7.3	mA
	+5 dBm output power setting 2440 MHz	9.6	mA

6. MSL & ESD

Table 13: MSL and ESD

Parameter	Test Conditions		Value
MSL grade:	MSL 3(1)		
ESD grade:	Human body model (HBM), per ANSI/ESDA/JEDEC JS001(2)	All pins	±2000V
	Charged device model (CDM), per JESD22-C101(3)	All pins	±500V

(1)The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the Picture below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the Picture below, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Notice (注意) :

Feasycom module must use Step-Stencil, suggestion using the stencil thickness about 0.16-0.2mm, it could be modify with the product.

使用我司模块，须使用阶梯钢网，建议阶梯钢网厚度 0.16-0.20mm，可根据自己产品适应性，进行相应调整.

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Table 14: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

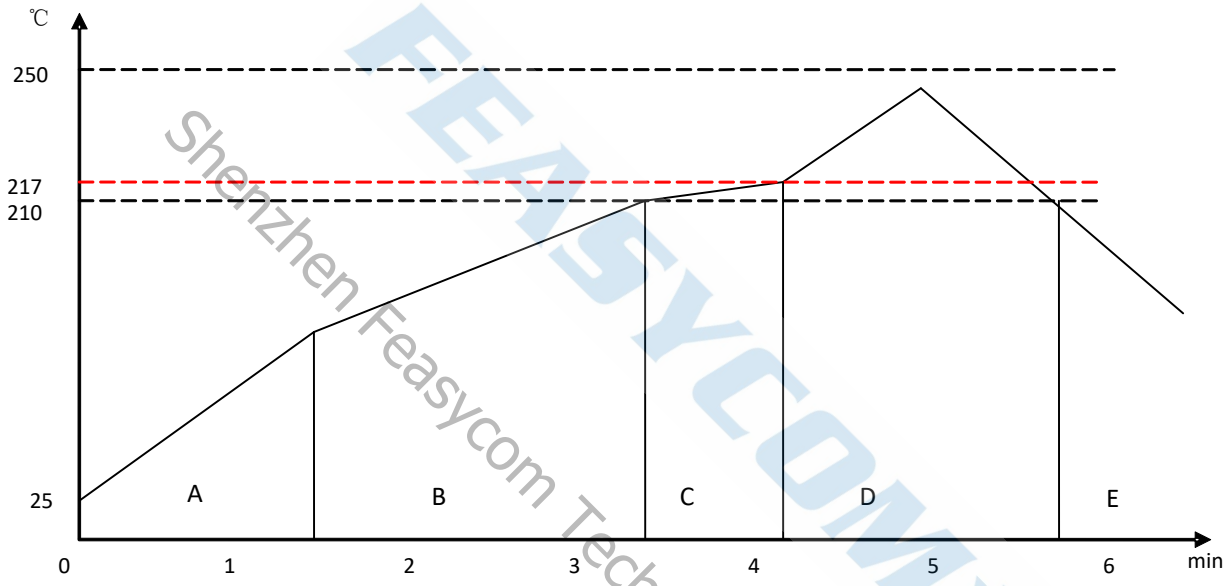

Figure 10: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

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8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 13mm(W) x 26.9mm(L) x 2.0 mm(H) Tolerance: ±0.2mm
- Module size: 13mm X 26.9mm Tolerance: ±0.2mm
- Pad size: 1mmX0.8mm Tolerance: ±0.1mm
- Pad pitch: 1.5mm Tolerance: ±0.1mm

(分板后边角残留板边误差：不大于0.5mm)

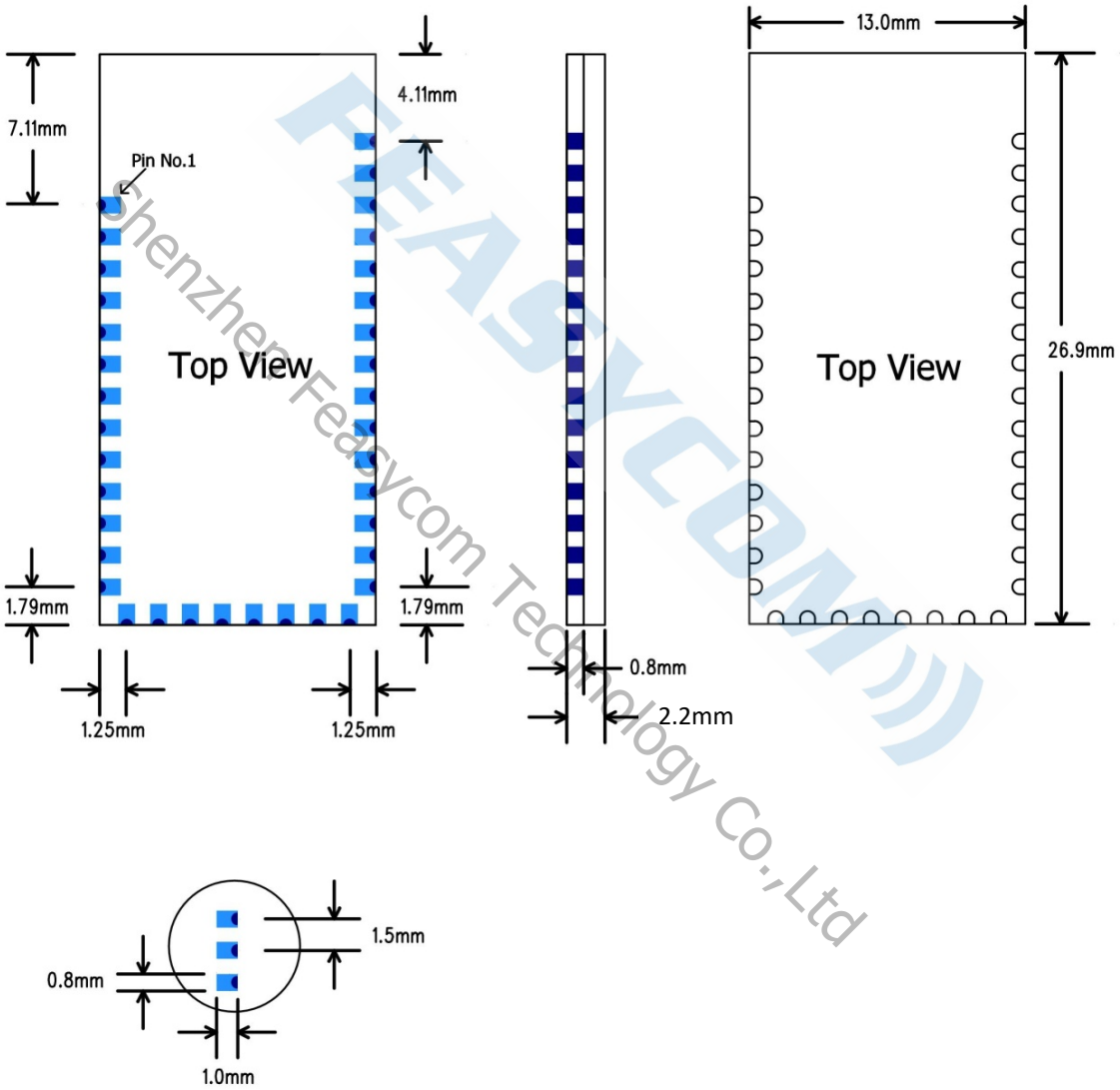

Figure 11: FSC-BT618V footprint

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8.2 Host PCB Land Pattern and Antenna Keep-out for FSC-BT618V

Please check the picture below for Pad Structure and Keep Out Area:

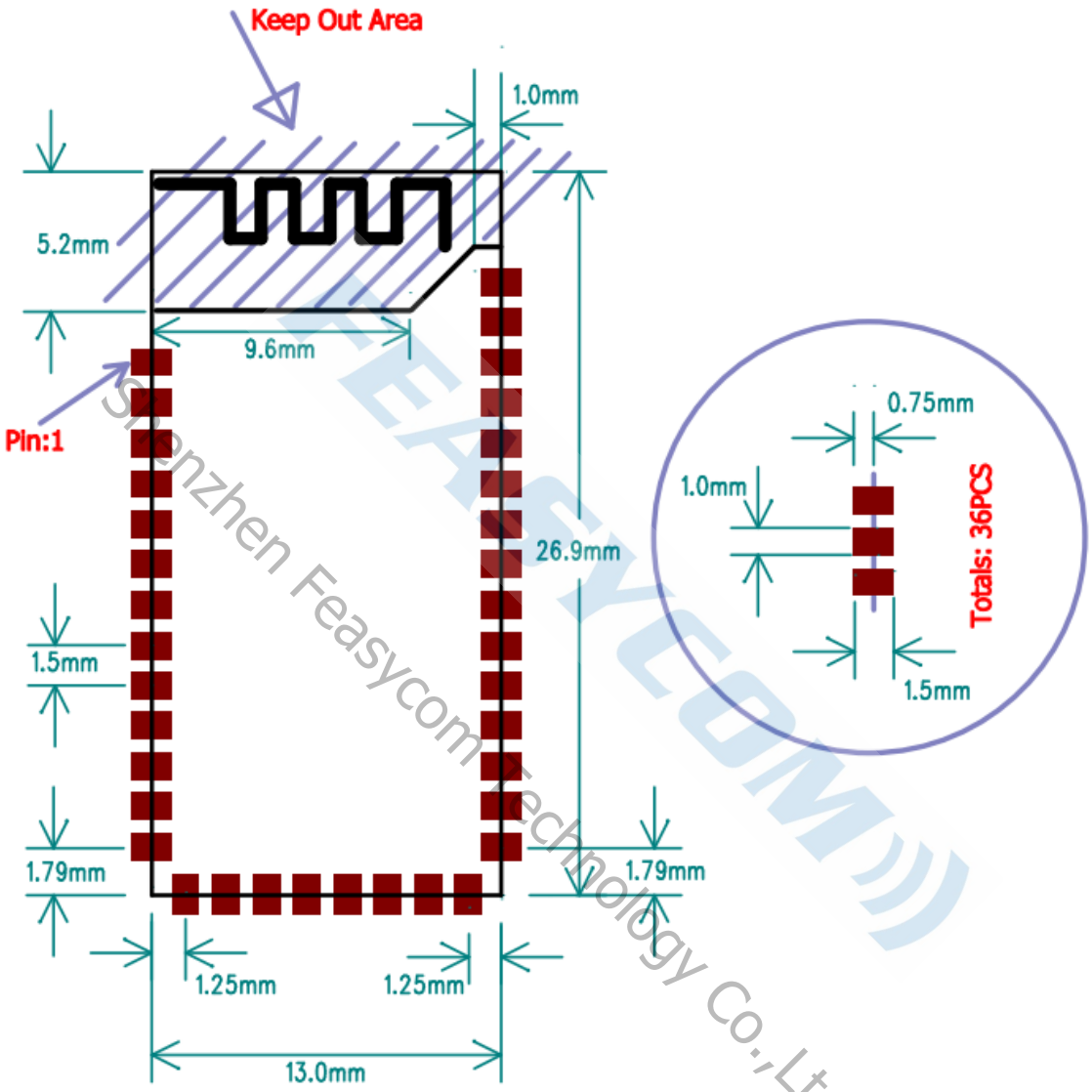

Figure 12: Host PCB-Top View

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BT618V is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

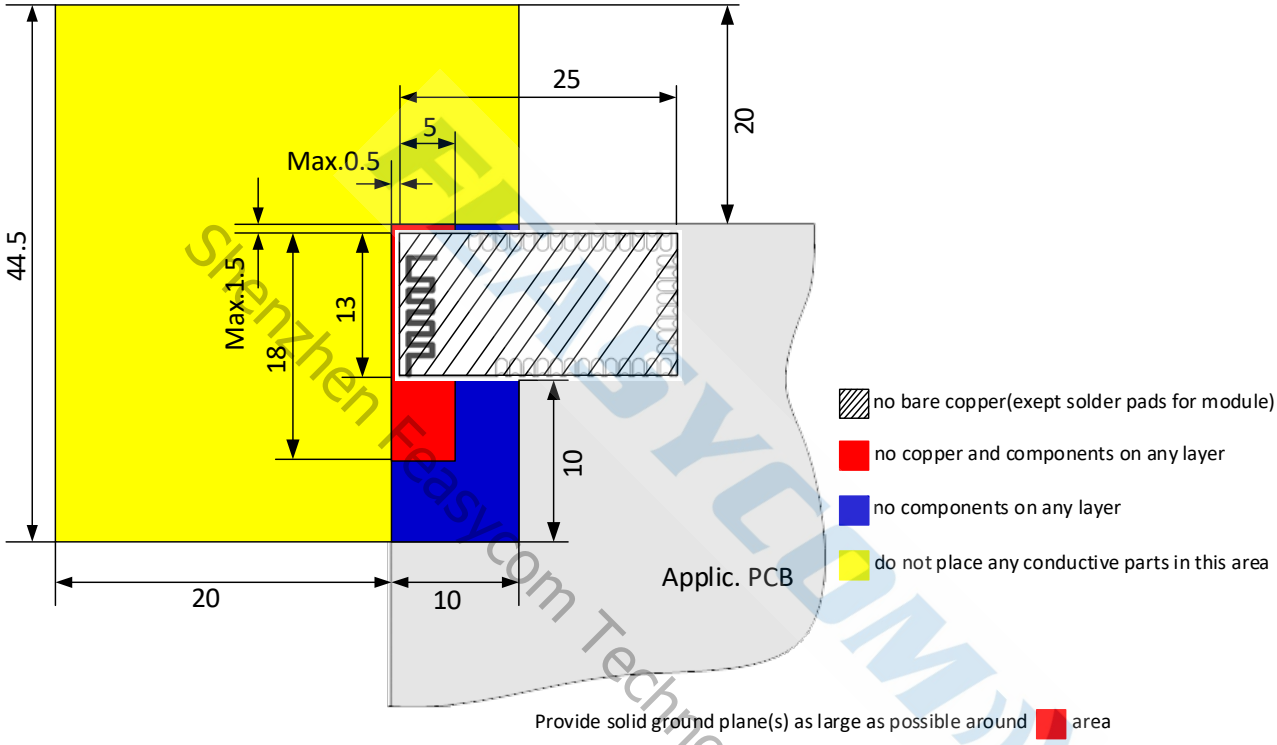

Figure 13: FSC-BT618V Restricted Area (Unit: mm)

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in picture below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

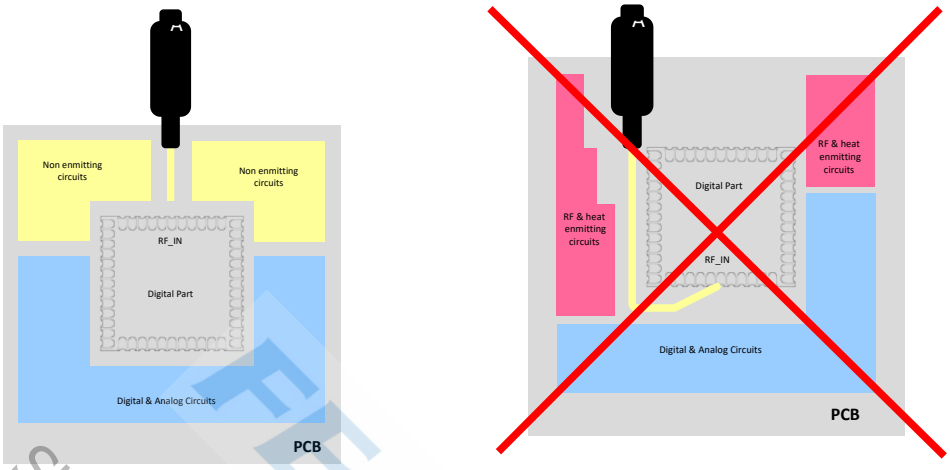

Figure 14: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

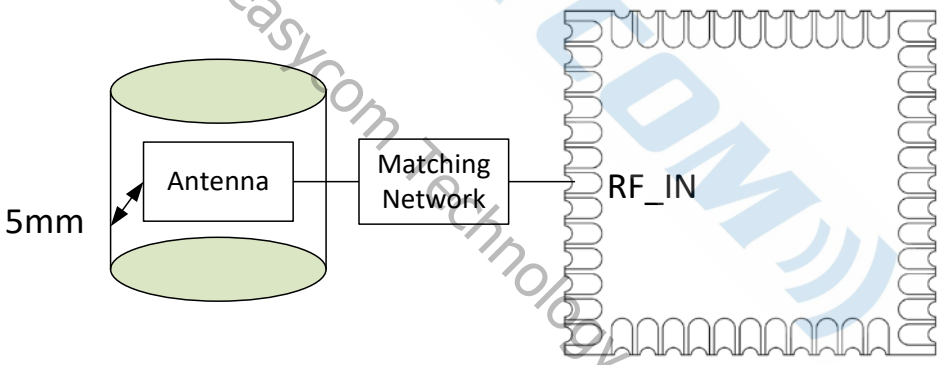

Figure 15: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

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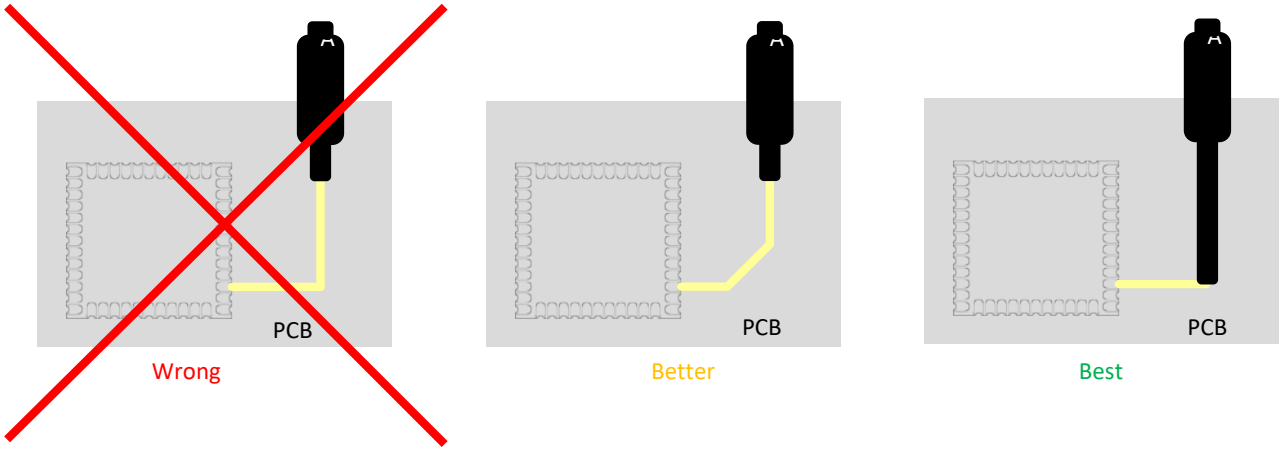


Figure 16: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

10. PRODUCT PACKAGING INFORMATION

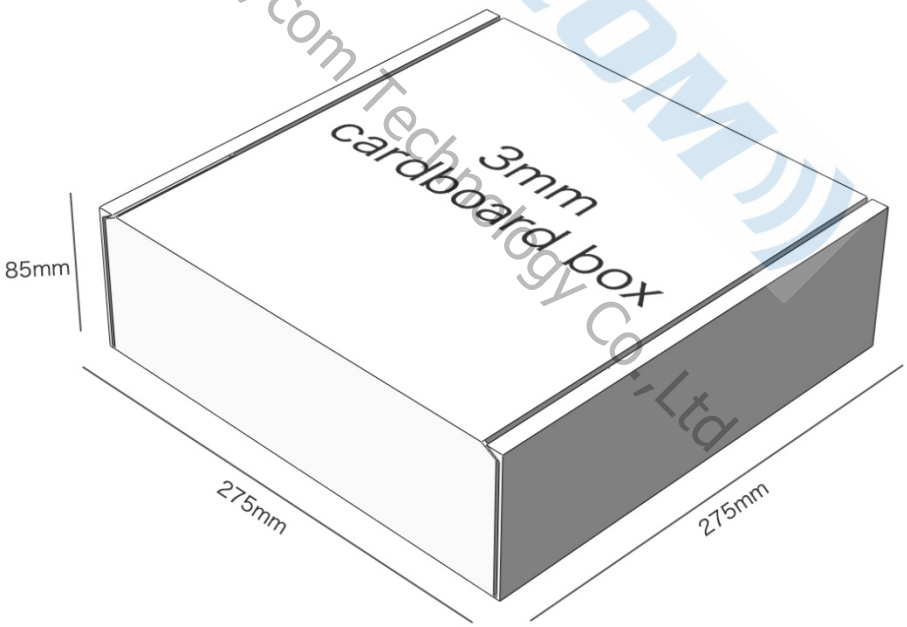
10.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 180mm * 195mm

Figure 17: Tray vacuum

10.2 Packing box(Optional)



* If require any other packing, must be confirmed with customer

* Package: 1000PCS Per Carton (Min Carton Package)

Figure 18: Packing Box

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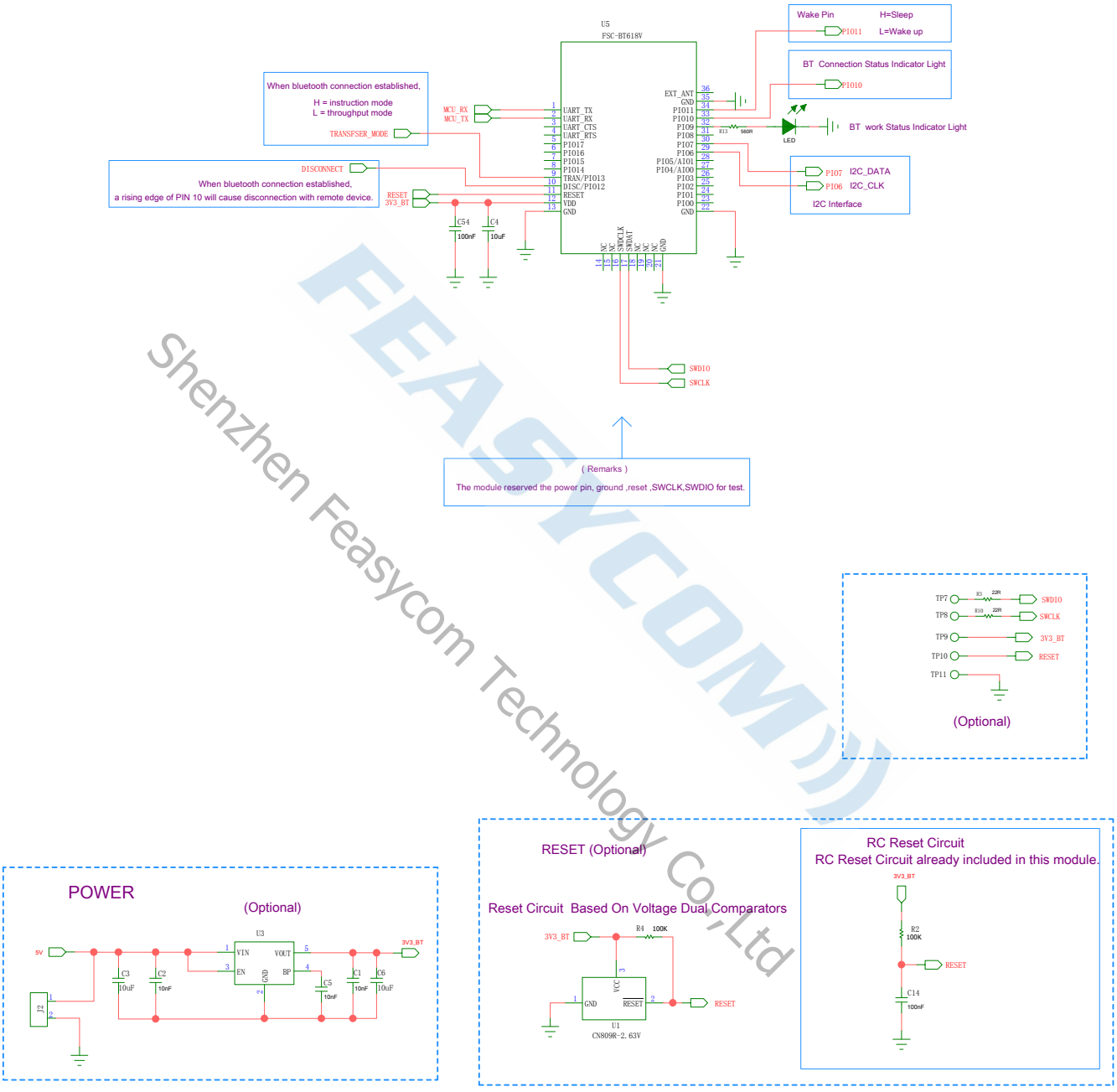
11. APPLICATION SCHEMATIC



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