
# FSC-BT3721V

DATASHEET V1.1

## Revision History

| Version | Data | Notes | Author |
|---|---|---|---|
| V1.0 | 2024-03-7 | Initial Version | Xianjian Mo |
| V1.1 | 2024-03-27 | Change the operating temperature and operating voltage | Xianjian Mo |



## Contact Us

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# 1 INTRODUCTION

## Overview

The FSC-BT3721V supports Bluetooth 5.3 network (BLE), an Internet of Things devices and meets the requirements of AEC-Q 100 standard. By default, the FSC-BT3721V module is flashed with Feasycom firmware, which is powerful and user-friendly. It's easy to use and completely encapsulated. Feasycom firmware enables users to access Bluetooth functionality through simple ASCII commands sent to the modules over a serial interface - it's just like a Bluetooth modem. As a result, FSC-BT3721V provides an ideal solution for developers who want to integrate Bluetooth wireless technology into their design.

## Features

- **Low Power Wireless System-on-Chip**
  - 32-bit ARM® Cortex®-M33 core with 76.8MHz maximum operating frequency
  - Up to 512 kB of flash and 32 kB Of RAM
  - Energy-efficient radio core with low active and sleep currents
  - Bluetooth 5.3 Direction Finding
  - Integrated PA with up to 6 dBm (2.4 GHz)TX power
  - Secure Boot with Root of Trust and Secure Loader (RTSL)
  - 2.4 GHz radio operation
- **Radio Performance**
  - -106.7 dBm sensitivity @ 125 kbps GFSK
  - -98.9 dBm sensitivity @ 1 Mbit/s GFSK
  - -96.2 dBm sensitivity @ 2 Mbit/s GFSK
  - TX power up to 6 dBm
  - 2.5 mA radio receive current
  - 3.4 mA radio transmit current @ 0 dBm output power
  - 7.5 mA radio transmit current @ 6 dBm output power
- **Low System Energy Consumption**
  - 3.6 mA RX current (1 Mbps GFSK)
  - 4.1 mA TX current @ 0 dBm output power
  - 8.2 mA TX current @ 6 dBm output power
  - 27 μA/MHz in Active Mode (EM0) at 76.8 MHz
  - 1.40 μA EM2 Deep Sleep current (32 kB RAM retention and RTC running from LFXO)
  - 1.75 μA EM2 Deep Sleep current (32 kB RAM retention and RTC running from Precision LFRCO)
  - 0.17 μA EM4 current
- **Supported Modulation Format**
  - 2 (G)FSK with fully configurable shaping
  - OQPSK DSSS
  - (G)MSK
- **Supported Protocols**
  - Bluetooth Low Energy (Bluetooth 5.3)
- • Direction finding using Angle-of-Arrival (AoA) and Angle-of-Departure (AoD)

- Proprietary

### Applications

- Tags and Beacons of Assets
- Consumer Electronics Remote Controls
- Portable Medical
- Bluetooth Mesh Low Power Nodes
- Sports, Fitness, and Wellness devices
- Connected Home
- Building Automation and Security
- Automotive Applications



# 2 GENERAL SPECIFICATIONS

Table 2-1：General Specifications

| Categories | Features | Implementation |
|---|---|---|
| Bluetooth | | |
| | Chip model | SILICON LABS EFR32BG22 |
| | Bluetooth Standard | Bluetooth Low Energy (Bluetooth 5.3) |
| | Frequency Band | 2402MHz ~ 2480MHz |
| | Interface | UART/SPI/PIO/ADC |
| | Transmit Power | +6 dBm (Max.) |
| | Receiver | -98 dBm sensitivity @ 1 Mbit/s GFSK |
| Size | | 16.6mm × 13.7 mm × 2.3mm |
| Operating temperature | | -40°C ~+85°C |
| Storage temperature | | -40°C ~+125°C |
| Supply Voltage | | 1.75V~3.8V |
| Miscellaneous | Lead Free<br>Warranty | Lead-free and RoHS compliant<br>One Year |
| Humidity | | 10% ~ 90% non-condensing |
| MSL grade: | | MSL 3 |
| ESD grade: | | Human Body Model: Pass ±2000 V,<br>Charge device model: Pass ±500 V, |
| | | |

# 3 HARDWARE SPECIFICATIONS

## 3.1 Block Diagram and PIN Diagram

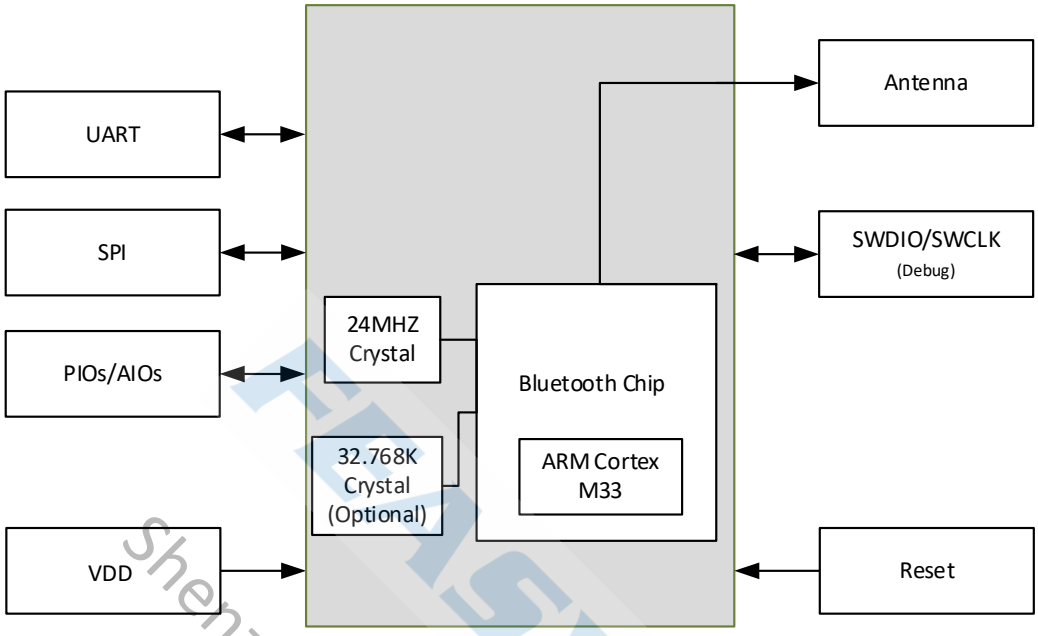


Figure 3-1-1: FSC-BT3721V Block Diagram

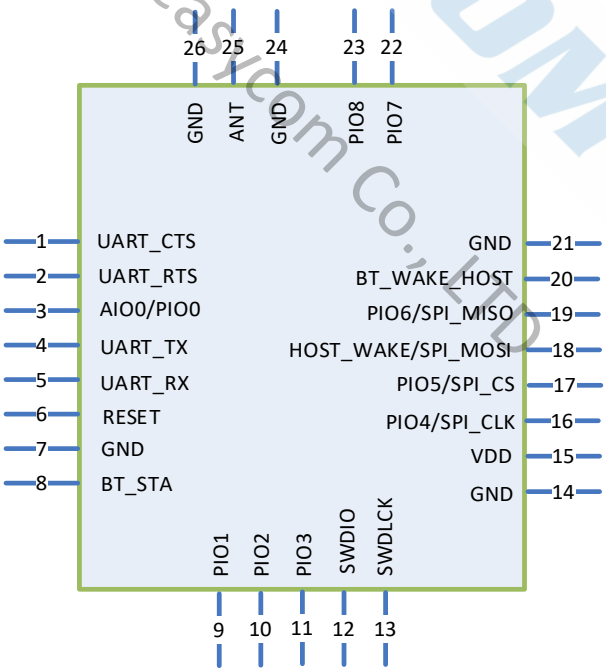


Figure 3-1-2: FSC-BT3721V PIN Diagram (Top View)

## 3.2 PIN Definitions

Table 3-2：Pin definitions

| Pin | Pin Name | Type | Pin Descriptions | Notes |
|---|---|---|---|---|
| 1 | UART_CTS | I/O | UART_CTS<br>Alternative function 1: Programmable I/O | |
| 2 | UART_RTS | I/O | UART_RTS<br>Alternative function 1: Programmable I/O | |
| 3 | AOI0/PIO0 | I/O | ADC<br>Alternative function 1: Programmable I/O | |
| 4 | UART_TX | O | UART_TX | |
| 5 | UART_RX | I | UART_RX | |
| 6 | RESET | I | RESET<br>System rest input with pull high, low active with low to trigger system rest | |
| 7 | GND | Vss | Power Ground | |
| 8 | BT_STA | I/O | BT status: Bluetooth unconnected output low, Bluetooth connected output high | |
| 9 | PIO1 | I/O | Programmable I/O | |
| 10 | PIO2 | I/O | Programmable I/O | |
| 11 | PIO3 | I/O | Programmable I/O | |
| 12 | SWDIO | I/O | DEBUG: SWDIO | |
| 13 | SWDCLK | I | DEBUG: SWDCLK | |
| 14 | GND | Vss | Power Ground | |
| 15 | VDD | VDD | 3V3 Power input | |
| 16 | PIO4/SPI_CLK | I/O | Programmable I/O<br>Alternative function 1:SPI_CLK | |
| 17 | PIO5/SPI_CS | I/O | Programmable I/O<br>Alternative function 1:SPI_CS | |
| 18 | HOST_WAKE/SPI_MOSI | I/O | HOST _WAKE: Output high level to notify the host to sleep, Output low level to wake up the host<br>Alternative function 1:SPI_MOSI<br>Alternative function 2:Programmable I/O | |
| 19 | PIO6/SPI_MISO | I/O | Programmable I/O<br>Alternative function 1:SPI_MISO | |
| 20 | BT_WAKE | I/O | BT_WAKE :Module sleep control ,Input the low-level wake module, Input high level control module to sleep<br>Alternative function 1:Programmable I/O | |
| 21 | GND | Vss | Power Ground | |
| 22 | PIO7 | I/O | Programmable I/O | |
| 23 | PIO8 | I/O | Programmable I/O | |
| 24 | GND | Vss | Power Ground | |
| 25 | ANT | RF | Bluetooth transmit/receive | |
| 26 | GND | Vss | Power Ground | |

# 4 ELECTRICAL CHARACTERISTICS

## 4.1 UART Interface

The FSC-BT3721V UART interface features a standard 4-wire configuration comprising RX, TX, CTS, and RTS pins. It supports the H4 HCI interface. The default baud rate is set at 115.2k baud. To accommodate both high-speed and low-speed baud rates, the FSC-BT3721V offers options of multiple UART clocks.

Table 4-1：Possible UART Settings

| Parameter | Possible Values |
|---|---|
| Baud rate | Minimum - |
| | Standard 115200bps |
| | Minimum - |
| Flow control | Supports Automatic Flow Control (CTS and RTS lines) |
| Parity | None, Odd or Even |
| Number of stop bits | 1 |
| Bits per channel | 8 |

# 5 MSL & ESD

Table 5-1: MSL and ESD

| Parameter | Value |
|---|---|
| MSL grade: | MSL 3 |
| ESD grade | Electrostatic discharge |
| ESD – Human-body model (HBM) rating, JESD22-A114-F<br>(Total samples from one wafer lot) | Pass ±2000 V, all pins |
| ESD – Charge-device model (CDM) rating, JESD22-C101-D<br>(Total samples from one wafer lot) | Pass ±500 V, all pins |

# 6 RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to reflow, it is crucial to ensure that the modules are properly packaged to prevent moisture absorption. The new packages are equipped with desiccants to absorb moisture, and a humidity indicator card is included to indicate the moisture level maintained during storage and shipment. If the card indicates the need to bake the units, please refer to the instructions specified by IPC/JEDEC J-STD-033 and follow them accordingly. It is important to adhere to these instructions to prevent any potential moisture-related issues during the reflow process.

**Note:** The shipping tray should not be exposed to temperatures exceeding 65°C. If baking is necessary at higher temperatures indicated below, it is essential to remove the modules from the shipping tray. This precaution is important to avoid any potential damage or deformation to the tray caused by excessive heat.

Any module that exceeds its floor life but has not yet been manufactured should be repackaged by using new desiccants and humidity indicator cards. For devices with a Moisture Sensitivity Level (MSL) of 3, the floor life is 168 hours in an environment with 30℃/60%RH.

Floor life refers to the maximum allowable time a moisture-sensitive device can be exposed to ambient conditions without risking moisture absorption and potential damage during soldering.

*Notice (注意)：*

*The Feasycom's module must be used with a Step-Stencil. It is suggested to use a stencil thickness of approximately 0.16-0.2mm, which can be modified according to the product.*

**使用我司模块，须使用阶梯钢网，建议阶梯钢网厚度0.16-0.20mm，可根据自己产品适应性，进行相应调整.**

Table 6-1: Recommended baking times and temperatures

| MSL | 125°C Baking Temp. | | 90°C/≤ 5%RH Baking Temp. | | 40°C/ ≤ 5%RH Baking Temp. | |
|---|---|---|---|---|---|---|
| | Saturated @ 30°C/85% | Floor Life Limit + 72 hours @ 30°C/60% | Saturated @ 30°C/85% | Floor Life Limit + 72 hours @ 30°C/60% | Saturated @ 30°C/85% | Floor Life Limit + 72 hours @ 30°C/60% |
| 3 | 9 hours | 7 hours | 33 hours | 23 hours | 13 days | 9 days |

Feasycom surface mount modules are designed to facilitate easy manufacturing, including reflow soldering onto a PCB. However, it is the customer's responsibility to select the suitable solder paste and ensure that the oven temperatures during reflow meet the requirements specified by the solder paste manufacturer. Feasycom surface mount modules comply with the J-STD-020D1 standards for reflow temperatures.

The soldering profile may vary depending on different parameters, requiring a specific setup for each application. The data provided here is only intended as a general guideline for solder reflow and should be used as a reference.

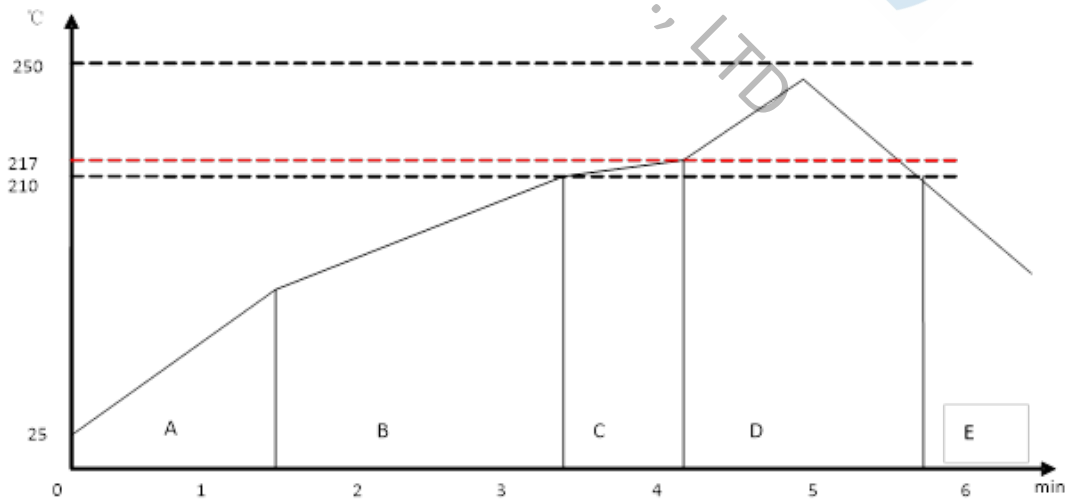


Figure6-1-1： Typical Lead-free Re-flow

**Pre-heat zone (A)** — This zone gradually increases the temperature at a controlled rate, usually **ranging from 0.5 to 2 °C/s**. Its purpose is to preheat the PCB board and components to a temperature of 120-150 °C. This stage is necessary to ensure the even distribution of heat across the PCB board and to remove any remaining solvents completely, minimizing the risk of heat shock to the components.

**Equilibrium Zone 1 (B)** — In this stage, the flux undergoes softening and uniformly covers the solder particles, as well as spreading over the PCB board. This process helps prevent re-oxidation of the solder particles. Additionally, as the temperature rises and the flux liquefies, each activator and rosin component become activated. They work together to eliminate any oxide film formed on the surface of the solder particles and PCB board. **For this zone, it is recommended to maintain a temperature range of 150 to 210 °C for a duration of 60 to 120 seconds.**

**Equilibrium Zone 2 (C) (optional)** — To address the issue of upright components, it is recommended to maintain a temperature range of 210 to 217 °C for a duration of approximately 20 to 30 seconds. This will help ensure proper soldering and alignment of the components on the PCB board.

**Reflow Zone (D)** — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

**Cooling Zone (E)** — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

# 7 MECHANICAL DETAILS

## 7.1 Mechanical Details

- Dimension: 16.6mm(W) x 13.7mm(L) x 2.3mm(H) Tolerance: ±0.2mm
- Module size: 16.6mm X 13.7mm Tolerance: ±0.2mm
- Pad size: 2.4mmX0.8mm Tolerance: ±0.2mm
- Pad pitch: 1.5mm Tolerance: ±0.1mm
- **(Residual plate edge error: < 0.5mm)**

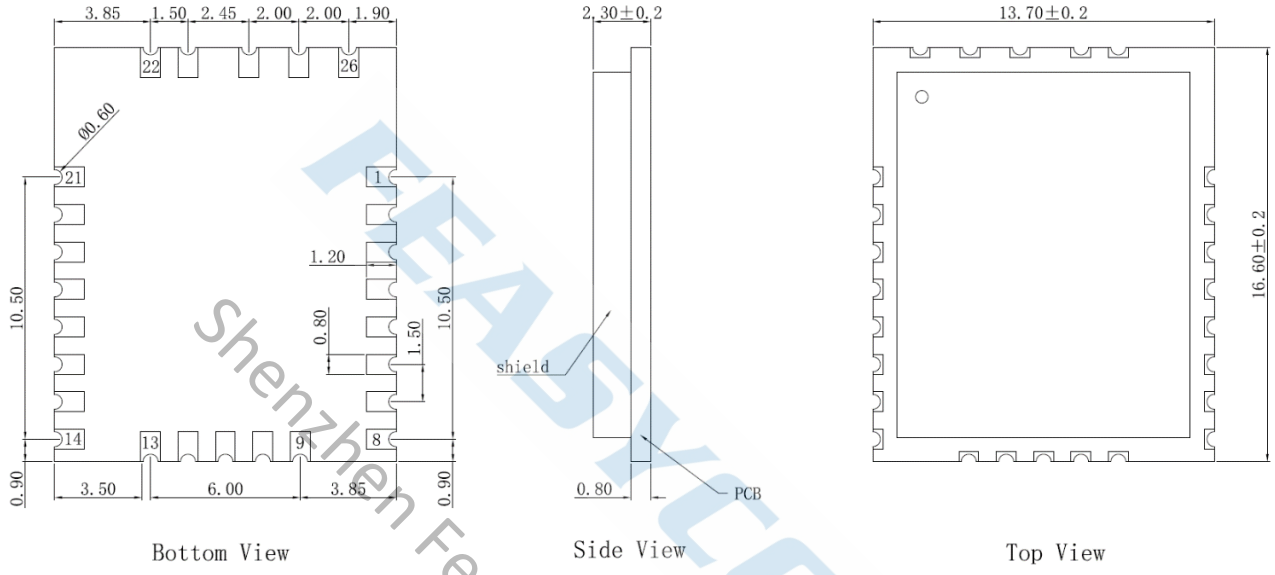


Figure 7-1-1: FSC-BT3721V footprint Layout Guide (Top View)

# 8 HARDWARE INTEGRATION SUGGESTIONS

## 8.1 Soldering Recommendations

FSC-BT3721V is compatible with the industrial standard reflow profile for Pb-free solders. The specific reflow profile used depends on factors such as the thermal mass of the populated PCB, heat transfer efficiency of the oven, and the type of solder paste used. It is advised to refer to the datasheet of the specific solder paste for profile configurations.

Feasycom provides the following recommendations for soldering the module to ensure reliable solder joints and proper module operation. However, since the optimal profile can vary based on the specific process and layout, these recommendations should be considered as a starting point guide and further study of the case is necessary.

## 8.2 Layout Guidelines (Internal Antenna)

It is strongly recommended to follow good layout practices in order to ensure proper operation of the module. Placing copper or any metal near the antenna can negatively impact its performance by affecting the matching properties. To prevent radiation, a metal shield should not be used with the module. It is advised to use grounding vias, spaced a maximum of 3 mm apart, at the edge of grounding areas to prevent RF penetration inside the PCB and unintentional resonator formation. Additionally, GND vias should be distributed all around the PCB edges.

In the restricted area where the on-board antenna is located, the motherboard should not have any bare conductors or vias. This area is not covered by stop mask print, so no copper (planes, traces, or vias) should be present in this area to avoid mismatching with the on-board antenna.

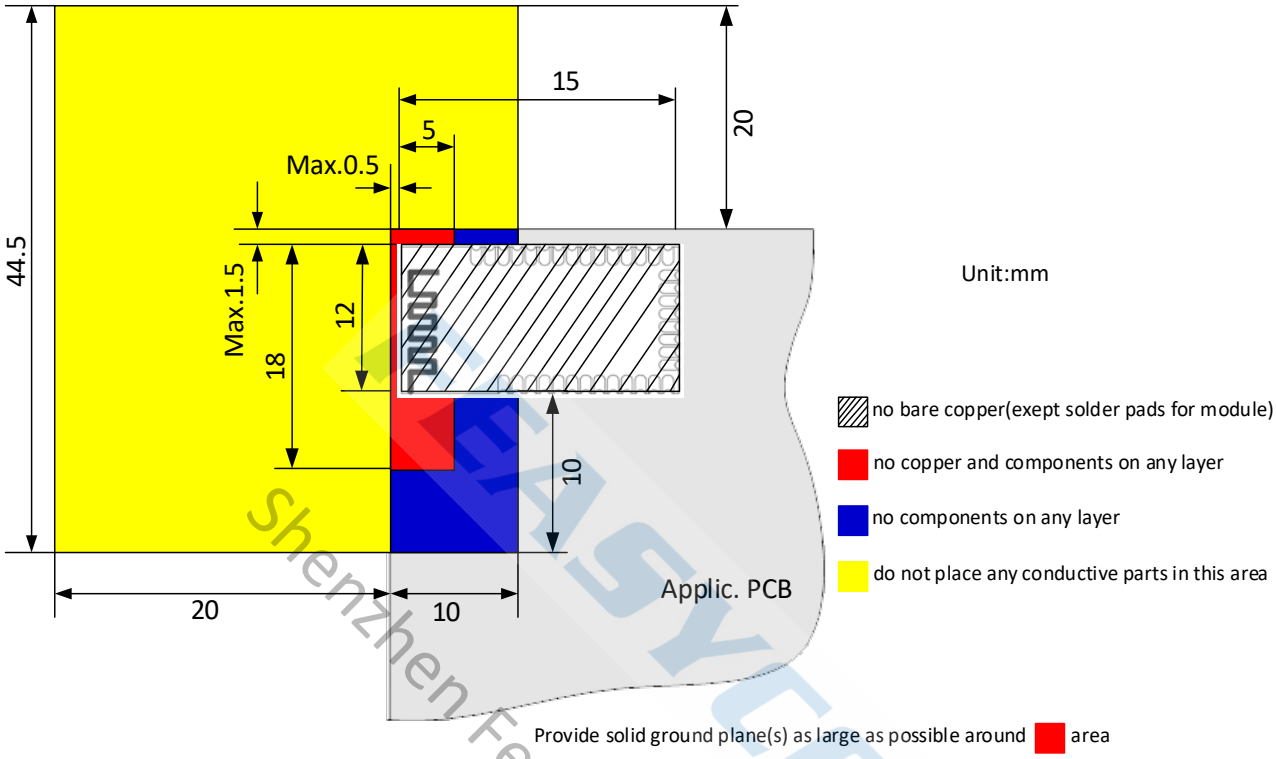


Figure 8-2-1：Restricted Area (Design schematic, for reference only. Unit: mm)

The following recommendations are aimed at avoiding EMC problems caused by the RF part of the module. It is important to note that each design is unique, and this list does not cover all basic design rules, such as avoiding capacitive coupling between signal lines. Additionally, it is crucial to consider potential problems arising from digital signals in the design.

To mitigate EMC issues, it is advisable to ensure that signal lines have return paths that are as short as possible. For instance, if a signal passes through a via to an inner layer, always use ground vias around it. These ground vias should be located tightly and symmetrically around the signal vias. Routing of sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area both above and below the line. If this is not feasible, make sure to keep the return path short by employing alternative methods, such as placing a ground line next to the signal line.

## 8.3 Layout Guidelines (External Antenna)

The placement and PCB layout play a critical role in optimizing the performance of modules without on-board antenna designs. The trace connecting the antenna port of the module to an external antenna should have a characteristic impedance of 50Ω and should be kept as short as possible to prevent interference into the transceiver of the module. When positioning the external antenna and RF-IN port of the module, it is important to keep them away from any sources of noise and digital traces. To minimize return loss and achieve better impedance matching, a matching network may be required between the external antenna and RF-IN port.

To ensure proper RF performance, it is recommended to clearly separate the RF critical circuits of the module from any digital circuits on the system board. The RF circuits within the module are located near the antenna port. Therefore, the module should be placed in such a way that the module's digital part faces the digital section of the system PCB.

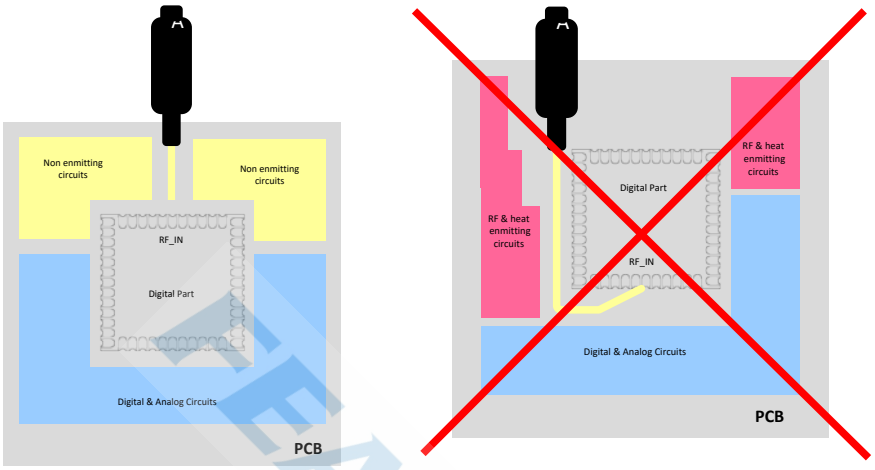


Figure 8-3-1: Placement the Module on a System Board

### 8.3.1 Antenna Connection and Grounding Plane Design

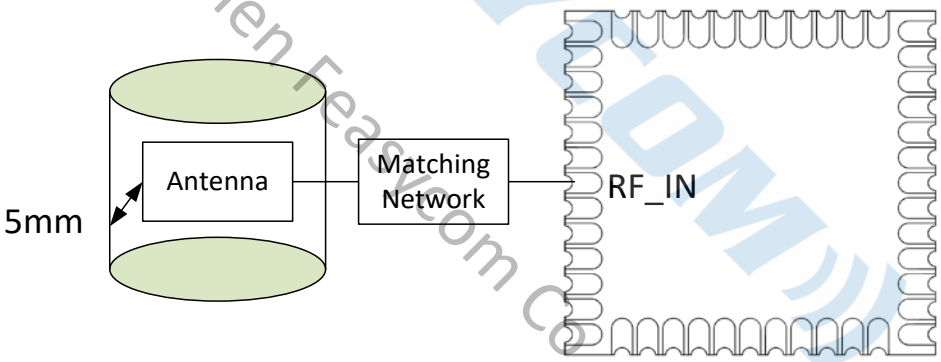


Figure 8-3-1-1: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should be at least as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

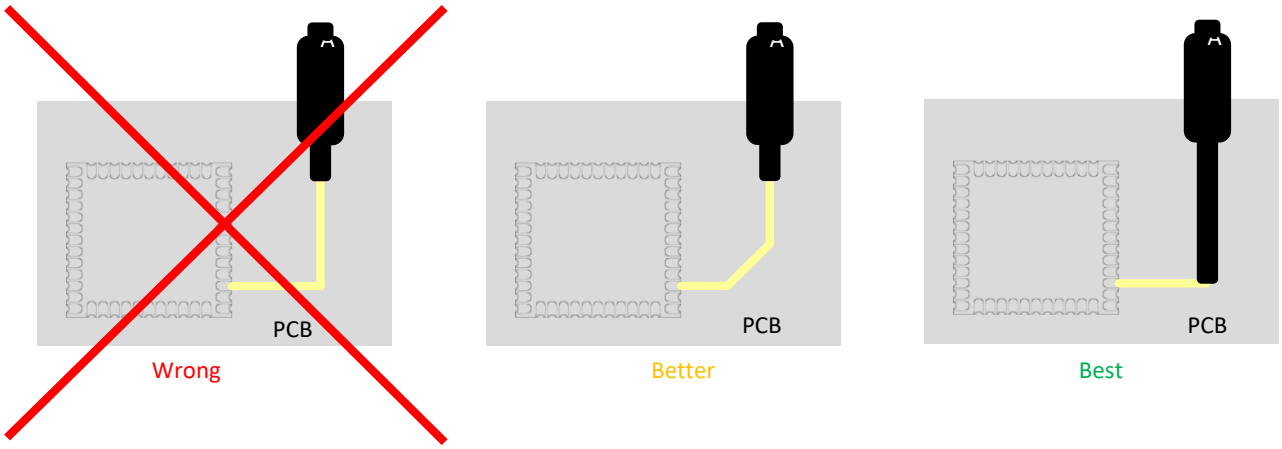


Figure 8-3-1-2: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

# 9 PRODUCT PACKAGING INFORMATION

## 9.1 Default Packing

Figure 9-1-1: Tray vacuum

## 9.2 Packing box (Optional)

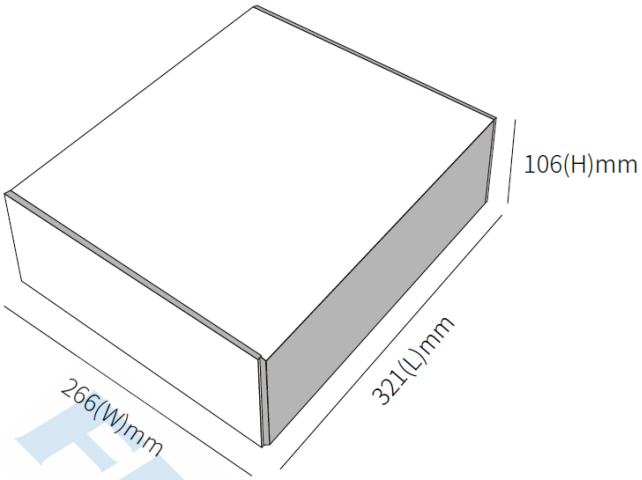


Figure 9-2-1: Packing box (Optional)

** If any packaging other than the package mentioned above is required, please confirm the packaging size again..*

** Packing: 1000pcs per carton (Minimum packing quantity).*

** The outer packing size provided above is for reference purposes only. For the actual dimensions of the product's packaging, please refer to the packaging of the actual goods.*

# 10 APPLICATION SCHEMATIC