FSC-UM8321

DATASHEET V1.0

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Revision History

Version	Data	Notes	Author
V1.0	2023-08-26	Initial Version	Lu zhu

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1 INTRODUCTION

Overview

The FSC-UM8321 is a fully integrated UWB transceiver module based on the Qorvo DW3220 IC. Integration of the DW3220 IC, nRF52840 MCU, planar UWB antenna, accelerometer, power management and crystal simplify the design cycle. The RF design is fully validated, tested, and calibrated. Low power consumption allows powering from batteries for extended periods, providing cost-effective implementation of UWB solutions. The FSC-UM8321 can be used in two-way ranging and TDoA applications. The FSC-UM8321 is designed to be compliant to the FiRa TM PHY and MAC specifications enabling interoperability with other FiRaTM compliant devices.

Features

IEEE 802.15.4-2015 and IEEE 802.15.4z BPRF compliant

Fully aligned with FiRa TM PHY, MAC and certification development

Supports Channels 5 (6.5 GHz) and 9 (8 GHz)

FCC, SRRC and ETSI certification (planned)

Nordic nRF52840 SoC with BLE transceiver

Bluetooth chip antenna

AES 128/256 Security block

Fully coherent receiver for maximum range and accuracy

Power consumption optimized for battery applications

Data rates of 850 kbps, 6.8 Mbps

Maximum packet length of 1023 bytes for high data throughput applications Integrated MAC support features

Backward compatible with the DWM1001C module

Application

Precision real time location systems (RTLS) using two-wayranging or TDoA schemes in a variety of markets.

Location aware wireless sensor networks (WSNs)

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2 General Specification

Table 2-1： General Specifications

Categories	Features	Implementation
Bluetooth		
	Bluetooth Standard	Bluetooth v5.2
	Frequency Band	2402MHz~2480MHz
	Transmit Power	-20 dBm ~ +8 dBm
	Receiver	-93dBm
	Interface	UART/I2C
UWB		
	UWB Standard	IEEE802.15.4-2015 UWB IEEE802.15.4z (BPRF mode)
	Frequency Band	Supports channels 5 & 9 (6489.6MHz & 7987.2 MHz)
	Data rates	Data rates of 850 kbps and6.8 Mbps
	Support	TDoA and TWR
Size	W x L x H	27.1mm×19.1mm×1.8mm(Height excluding shielding case) 27.1mm×19.1mm×2.4mm(Height including shielding case)
Operating temperature		-40°C ~+85°C
Storage temperature		-40°C ~+85°C
Supply Voltage		2.5V-3.6V
Miscellaneous	Lead Free Warranty	Lead-free and RoHS compliant One Year
MSL grade:		MSL 3
ESD grade:		Human Body Model: Pass ±2000 V, Charge device model: Pass ±500 V,

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3 HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

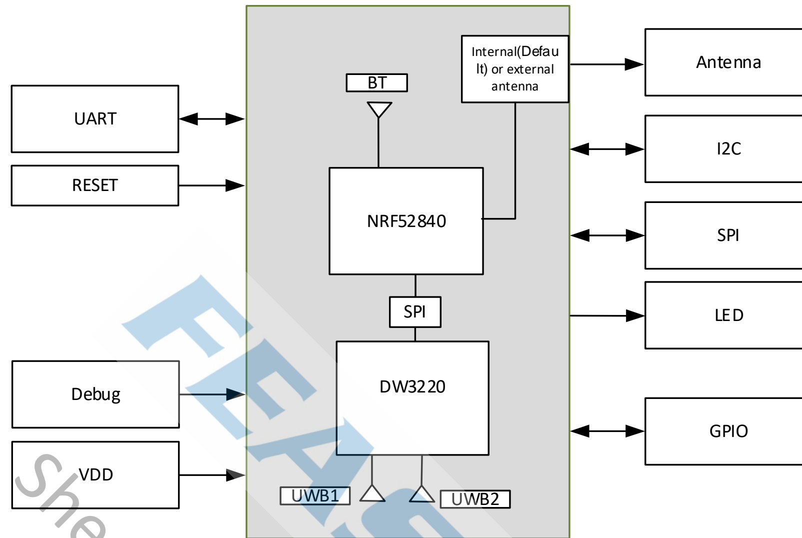

Figure 3-1:Block Diagram

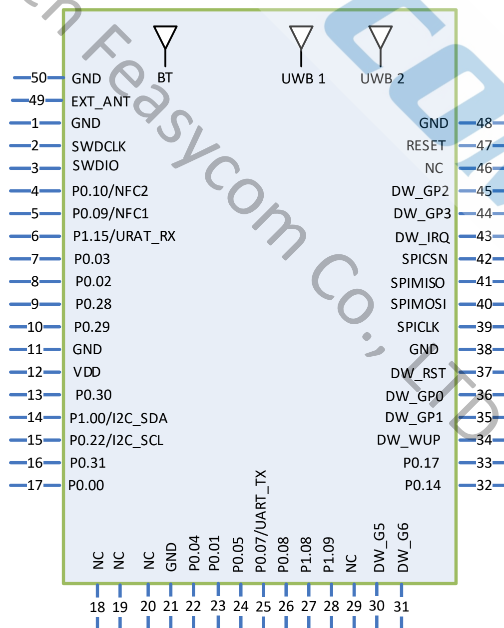

Figure 3-2:FSC-UM8321 PIN Diagram(Top View)

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3.2 PIN Definition Descriptions

Table 3-2： Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	GND	Vss	Power Ground	
2	SWCLK	I/O	Debug function: SWCK	
3	SWDIO	I/O	Debug function: SWDIO	
4	P0.10/NFC2	Mixed	Programmable I/O Debug function: NFC2	
5	P0.09/NFC1	Mixed	Programmable I/O Debug function: NFC1	
6	P1.15/UART_RX	I/O	Programmable I/O Alternative function:UART_RX	
7	P0.03	I/O	Programmable I/O	
8	P0.02	I/O	Programmable I/O	
9	P0.28	I/O	Programmable I/O	
10	P0.29	I/O	Programmable I/O	
11	GND	Vss	Power Ground	
12	VDD	VDD	3V3	
13	P0.30	I/O	Programmable I/O	
14	P1.00/I2C_SDA	I/O	Programmable I/O Alternative function: I2C_SDA	
15	P0.22/ I2C_SCL	I/O	Programmable I/O Alternative function: I2C_SCL	
16	P0.31	I/O	Programmable I/O	
17	P0.00	I/O	Programmable I/O	
18	NC			
19	NC			
20	NC			
21	GND	Vss	Power Ground	
22	P0.04	I/O	Programmable I/O	
23	P0.01	I/O	Programmable I/O	
24	P0.05	I/O	Programmable I/O	
25	P0.07/UART_TX	I/O	Programmable I/O	

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			Alternative function:UART_TX
26	P0.08	I/O	Programmable I/O
27	P1.08	I/O	Programmable I/O
28	PI.09	I/O	Programmable I/O
29	NC	I/O	Programmable I/O
30	DW_G5	I/O	Programmable I/O for DW3220 transceiver
31	DW_G6	I/O	Programmable I/O for DW3220 transceiver
32	P0.14	I/O	Programmable I/O
33	P0.17	I/O	Programmable I/O
34	DW_WUP	Vss	Programmable I/O Alternative function: DW3220 wake up
35	DW_GP1	I/O	Programmable I/O for DW3220 transceiver
36	DW_GP0	I/O	Programmable I/O for DW3220 transceiver
37	DW_RST	I	RESET for DW3220 Active low
38	GND	Vss	Power Ground
39	SPICLK	I/O	Programmable I/O Alternative function: SPICLK
40	SPIMOSI	I/O	Programmable I/O Alternative function: SPIMOSI
41	SPIMISO	I/O	Programmable I/O Alternative function: SPIMISO
42	SPICSN	I/O	Programmable I/O Alternative function: SPICSN
43	DW_IRQ	I/O	Programmable I/O for DW3220 transceiver
44	DW_GP3	I/O	Programmable I/O for DW3220 transceiver
45	DW_GP2	I/O	Programmable I/O for DW3220 transceiver
46	NC		
47	RESET	I	RESET for NRF52840 Active low
48	GND	Vss	Power Ground
49	EXT_ANT	O	RF signal output
50	GND	Vss	Power Ground

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4 MSL & ESD

Table 6-1: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade	Electrostatic discharge
ESD – Human-body model (HBM) rating, JESD22-A114-F (Total samples from one wafer lot)	Pass ±2000 V, all pins
ESD – Charge-device model (CDM) rating, JESD22-C101-D (Total samples from one wafer lot)	Pass ±500 V, all pins

5 RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Notice (注意) :

Feasycom module must use Step-Stencil, suggestion using the stencil thickness about 0.16-0.2mm,it could be modify with the product.

Table 7-1: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

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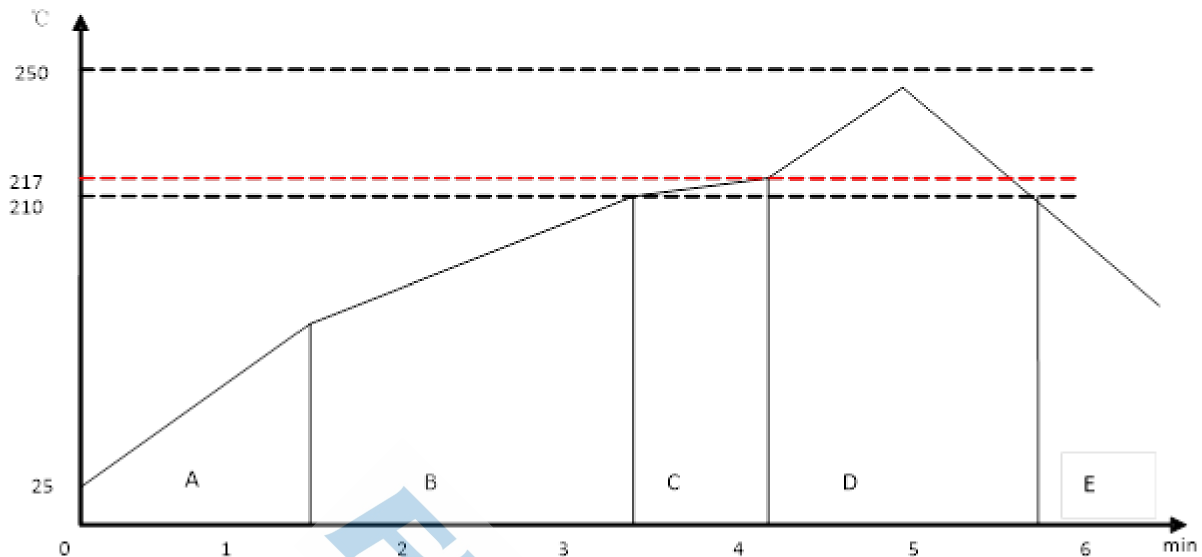

Figure 7-1: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

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6 MECHANICAL DETAILS

6.1 Mechanical Details

- Dimension: 19.1mm(W) x 27.1mm(L) x 2.4mm(H) Tolerance: ±0.2mm
- Module size: 19.1mm X 27.1mm Tolerance: ±0.2mm
- Pad size: 1mmX0.75mm Tolerance: ±0.2mm
- Pad pitch: 1mm Tolerance: ±0.1mm

(Residual plate edge error: < 0.5mm)

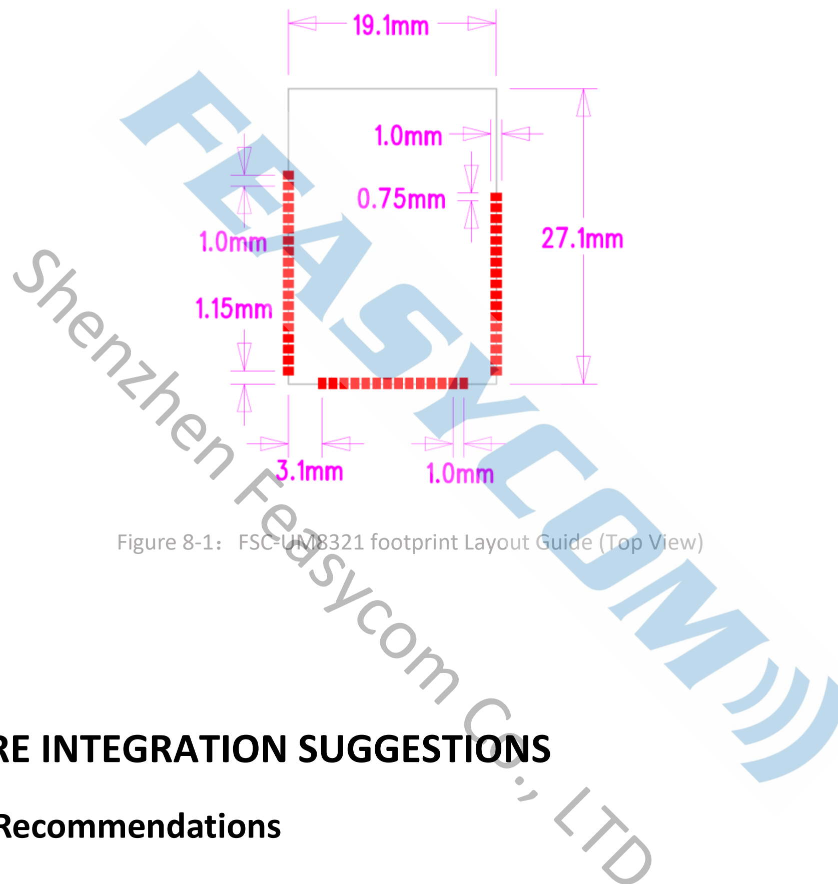

Figure 8-1：FSC-UM8321 footprint Layout Guide (Top View)

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7 HARDWARE INTEGRATION SUGGESTIONS

7.1 Soldering Recommendations

FSC-UM8321 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

7.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB

and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

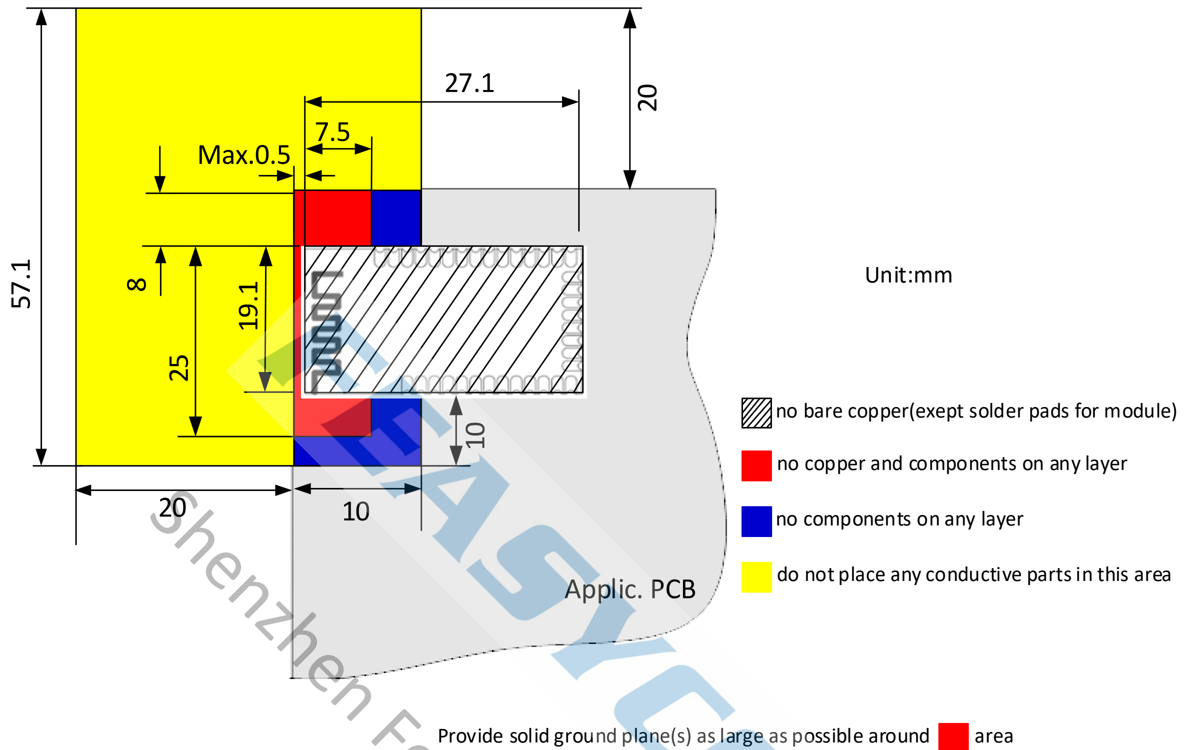

Figure 9-2： Restricted Area (Design schematic, for reference only. Unit: mm)

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

7.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed

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in this way that module digital part towards your digital section of the system PCB.

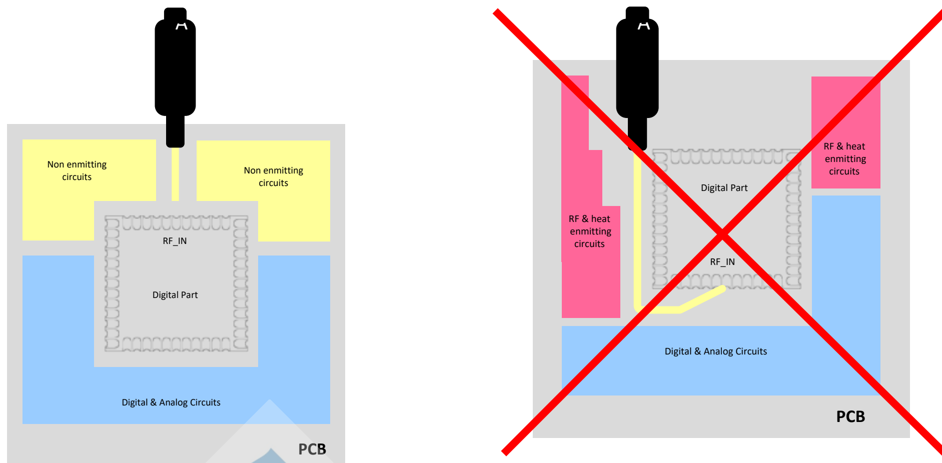

Figure 9-3: Placement the Module on a System Board

7.3.1 Antenna Connection and Grounding Plane Design

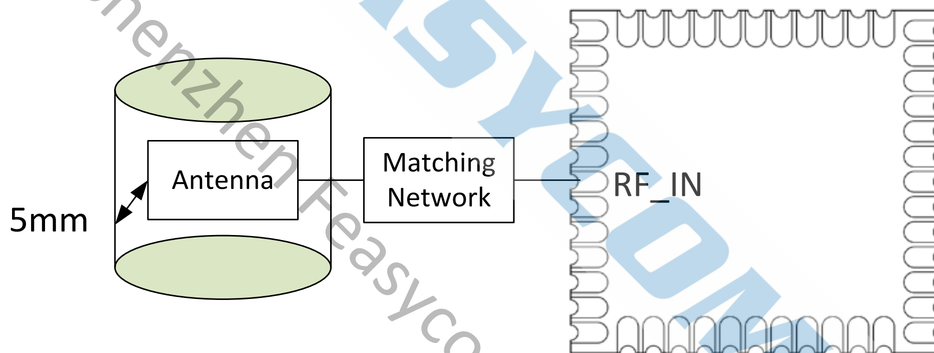

Figure 9-31-0: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

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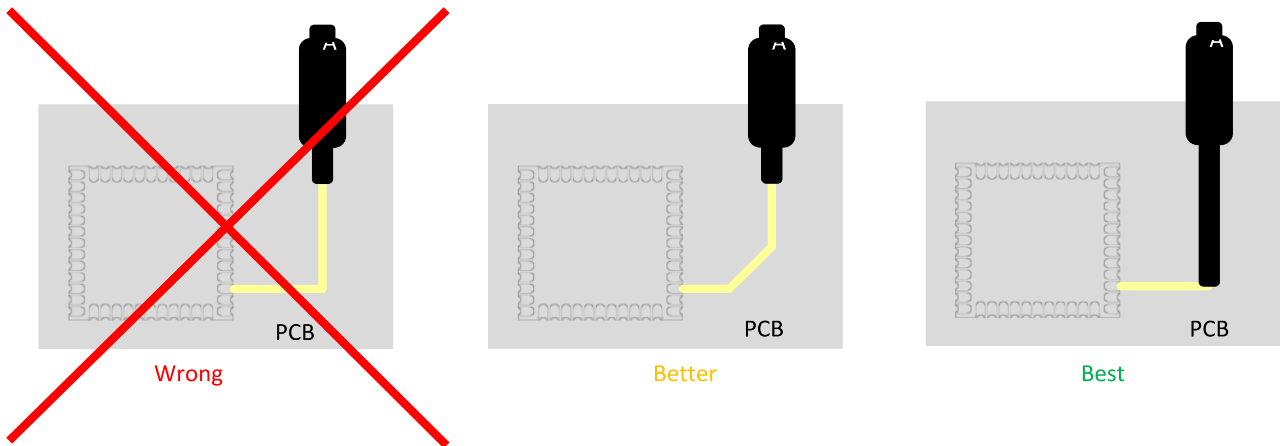

Figure 9-31-1: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many via as possible to connect the ground planes.

8 PRODUCT PACKAGING INFORMATION

8.1 Default Packing

Figure 10-1: Tray Dimension: 140mm * 265mm Tray vacuum

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8.2 Packing box(Optional)

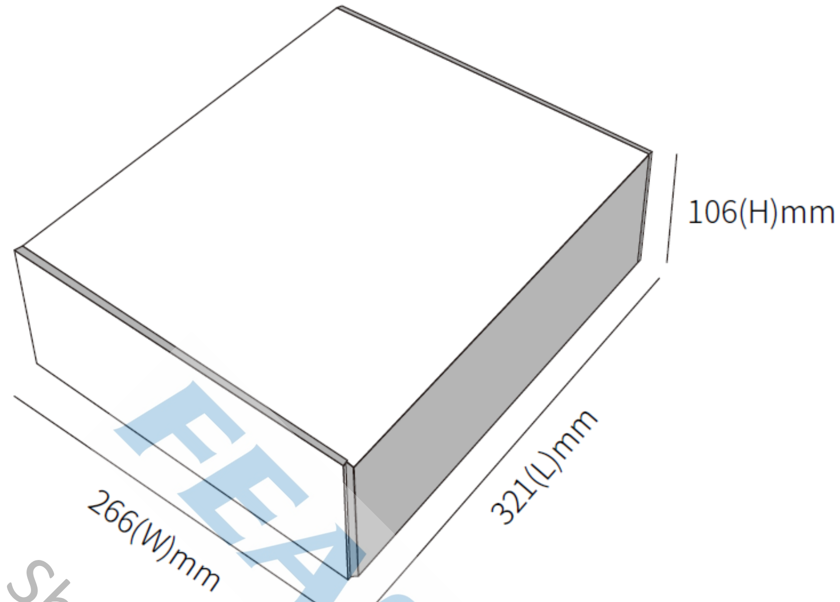

Figure 10-2: Packing box(Optional)

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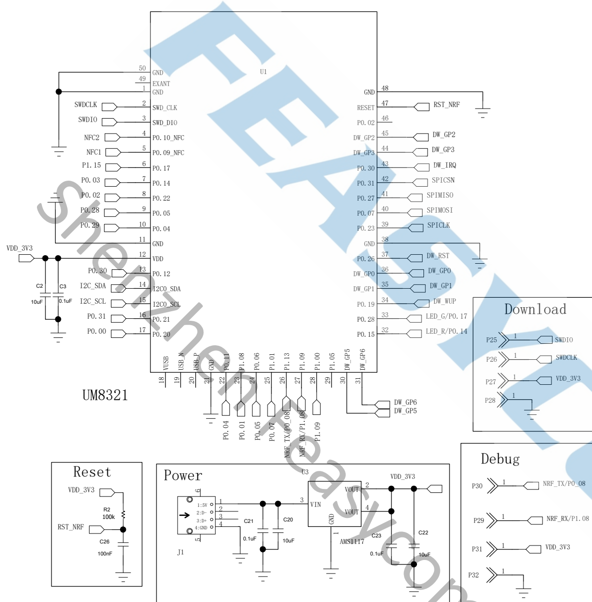
9 APPLICATION SCHEMATIC



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