FSC-BW3051

DATASHEET V1.0

Revision History

Version	Data	Notes	Author
V1.0	2023-08-12	Initial Version	leiyan Qin

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1 INTRODUCTION

Overview

FSC-BW3051 module integrates WLAN、BT/BLE in a single package module which support 802.11ac Wi-Fi 5 and Bluetooth (BT) v5.2. The Module is based on QCA6595 chipset of Qualcomm， the Module which uses the 112pins(around 76pins,bottom pads 36pins）23mm*23mm LGA package The module can be used for high-speed wireless connectivity of automotive information and entertainment systems.

WLAN Features

- Supports 802.11a/b/g/n/ac Wi-Fi5 compliant.
- Supports 2 × 2 Multi-User Multiple-Input Multiple-Output (MUMIMO).
- Supports Low power PCIE (w/L1 sub-state) interface.

Bluetooth Features

- Compliant with BT v5.2.
- Support LE Audio.
- High speed UART for BT，PCM/I2S for BT audio.

2 General Specification

Table 2-1：General Specifications

Categories	Features	Implementation
Bluetooth		
	Bluetooth Standard	Support Bluetooth 5.2+EDR
	Frequency Band	2.402G ~ 2.480G
	Interface	UART, PCM/I2S
	RF Input Impedance	50 ohms
WLAN		
	Frequency Band	2.4GHz/5GHz
	RF Input Impedance	50 ohms
	Interfaces	PCIE
operate condition		
	VDD_PMU	1.8V
	VDD2P2_1	2.2V
	VDD1V8_AON	1.8V
	VDDIO_3V3	3.3V
	Temperature	-40°C to +85°C

	Humidity	10%~90% Non-Condensing
Dimension		
	Dimension	23mm(L)*23mm(W)*2.9mm(H)
	weight	TBD
	coplanarity	<=0.1mm (ordinary temperature 25°C
	ROHS	ROHS2.0

3 HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

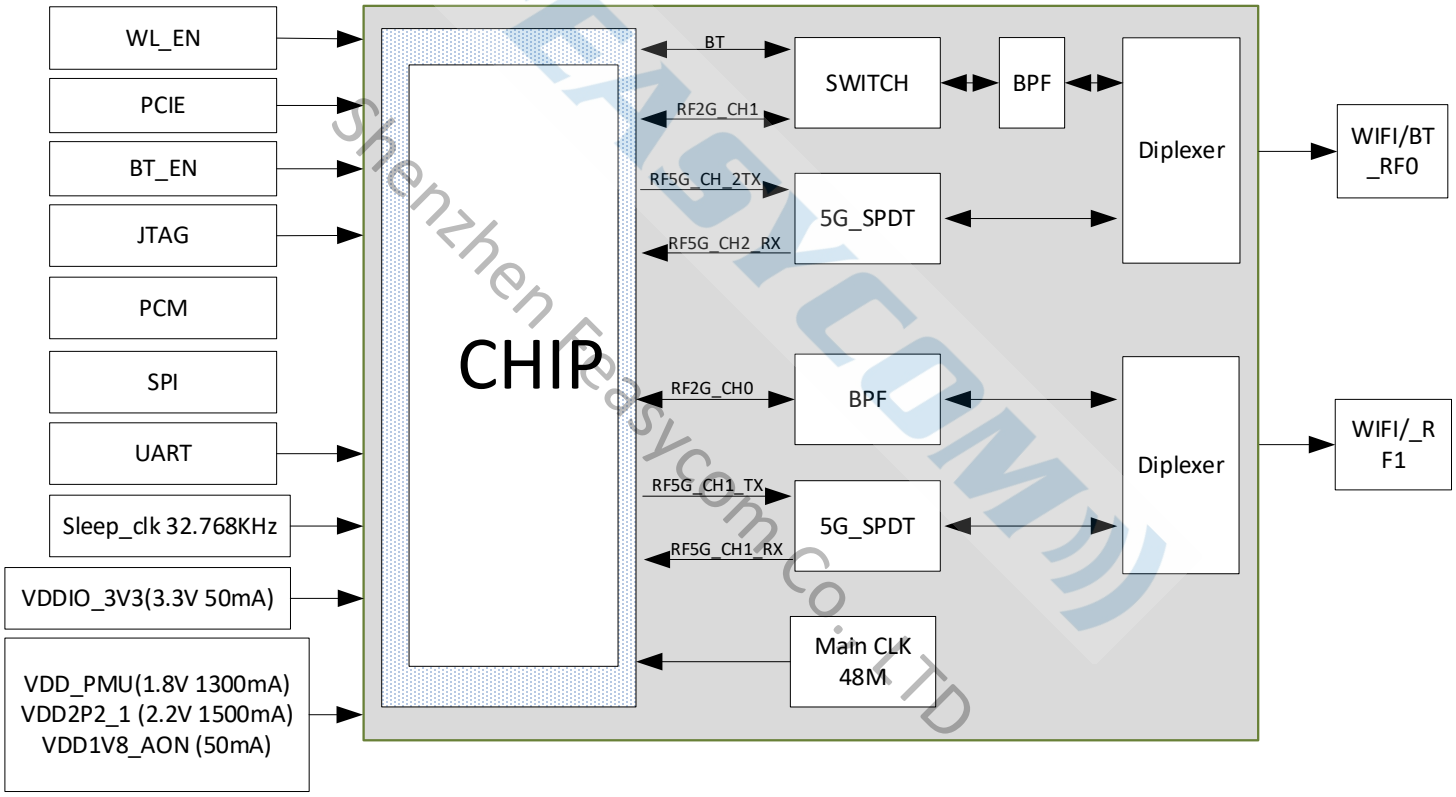


Figure 3-1-1: FSC-BW3051 Block Diagram

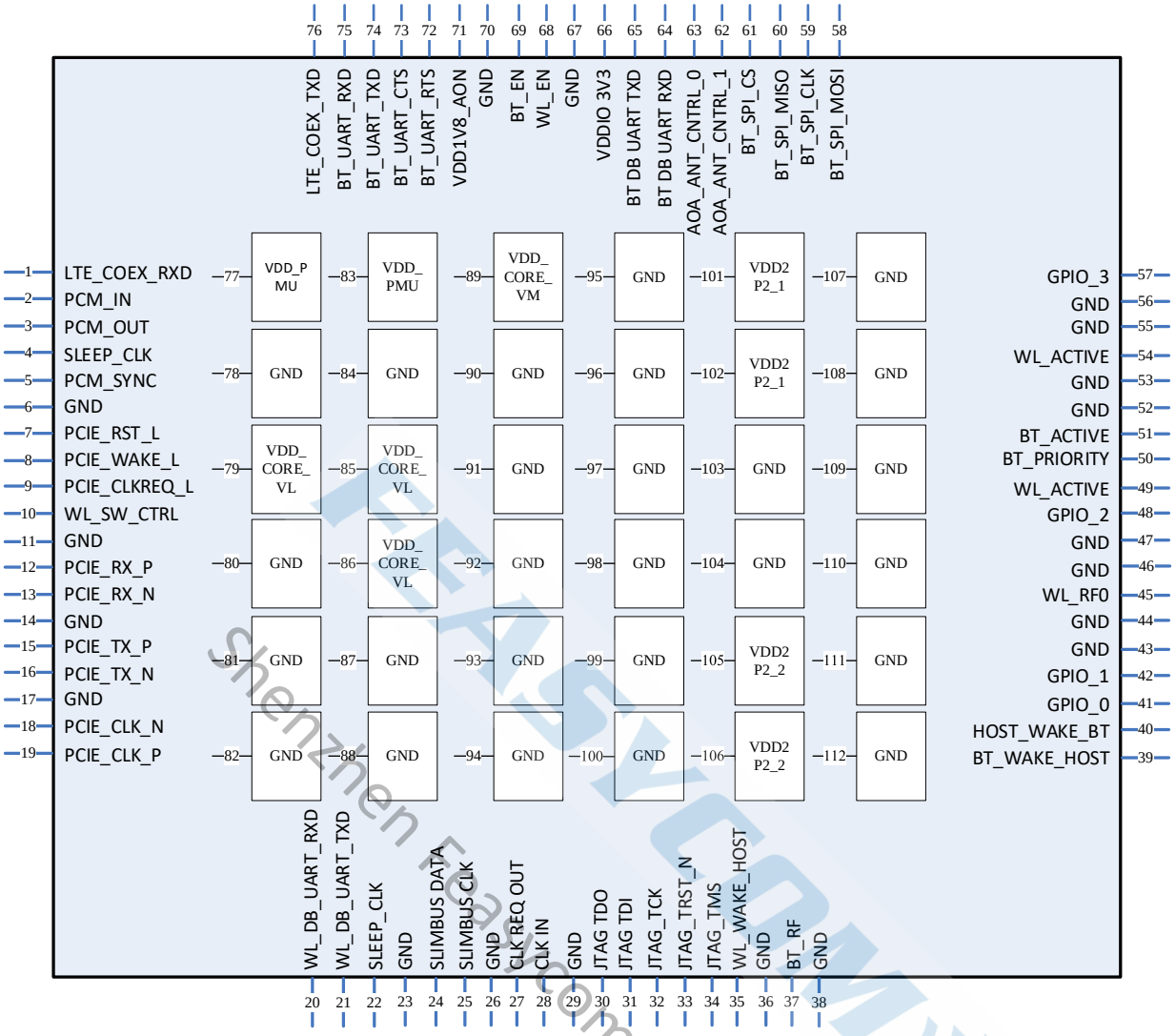


Figure 3-1-2: FSC-BW3051 PIN Diagram (Top View)

3.2 PIN Definition Descriptions

Table 3-2： Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	LTE_COEX_RXD	I	LTE coexistence UART RXD	
2	PCM_IN	I	BT PCM/I2S Bus Data in	
3	PCM_OUT	O	BT PCM/I2S Bus Data out	
4	PCM_CLK	I	BT PCM/I2S Bus Clock in	
5	PCM_SYNC	I	BT PCM/I2S Bus Frame sync BT	
6	GND	GND	Ground	
7	PCIE_RST_L	I	PCI express reset with weak pull-down	
8	PCIE_WAKE_L	O	Request to service a function -initiated Wake Event. (an external pull-up resistor to 1.8V is required)	
9	PCIE_CLKREQ_L	O	Reference clock request	

10	WL_SW_CTRL	F	Not Connected
11	GND	GND	Ground
12	PCIE_RX_P	I	PCI Express Receive Differential Pair
13	PCIE_RX_N	I	
14	GND	GND	Ground
15	PCIE_TX_P	O	PCI Express Transmit Differential Pair
16	PCIE_TX_N	O	
17	GND	GND	Ground
18	PCIE_CLK_N	I	PCI Express Differential Reference.
19	PCIE_CLK_P	I	
20	WL_DB_UART_RXD	F	Not Connected
21	WL_DB_UART_ TXD	F	Not Connected
22	SLEEP_CLK	I	Sleep clock input
23	GND	GND	Ground
24	SLIMBUS DATA	F	Not Connected
25	SLIMBUS CLK	F	Not Connected
26	GND	GND	Ground
27	CLK REQ OUT	O	Clock request output; NC if not used
28	CLK IN	I	If use TCXO, CLK input; NC if not used
29	GND	GND	Ground
30	JTAG TDO	O	Test data output (Reserved Point)
31	JTAG TDI	I	Test data input (Reserved Point)
32	JTAG_TCK	I	Test the clock (Reserved Point)
33	JTAG_TRST_N	I	Test reset (Reserved Point)
34	JTAG_TMS	I	Test mode selection (Reserved Point)
35	WL_WAKE_HOST	F	Not Connected
36	GND	GND	Ground
37	BT_RF	RF	Not Connected
38	GND	GND	Ground
39	BT_WAKE_HOST	O	Bluetooth wake up the host
40	HOST_WAKE_BT	F	Not Connected
41	GPIO_0	F	Not Connected
42	GPIO_1	F	Not Connected
43	GND	GND	Ground
44	GND	GND	Ground
45	WL_RF0	RF	WIFI 2.4G/5G RF and BT RF in/out port
46	GND	GND	Ground
47	GND	GND	Ground
48	GPIO_2	F	Not Connected

49	WL_ACTIVE	I/O	WLAN active
50	BT_PRIORITY	I/O	Bluetooth priority
51	BT_ACTIVE	I/O	BT active
52	GND	GND	Ground
53	GND	GND	Ground
54	WL_ACTIVE	I/O	WIFI 2.4/5GHz RF input/output port 1
55	GND	GND	Ground
56	GND	GND	Ground
57	GPIO_3	F	Not Connected
58	BT_SPI_MOSI	I	BT SPI MOSI (Master) (Reserved Point)
59	BT_SPI_CLK	I	BT SPI CLK (Master) (Reserved Point)
60	BT_SPI_MISO	O	BT SPI MISO (Master) (Reserved Point)
61	BT_SPI_CS	I	BT SPI CS (Master) (Reserved Point)
62	AOA_ANT_CNTRL_1	F	Not Connected
63	AOA_ANT_CNTRL_0	F	Not Connected
64	BT DB UART RXD	F	Not Connected
65	BT DB UART TXD	F	Not Connected
66	VDDIO 3V3	PI	3.3 V supply for VDD_RFSW
67	GND	GND	Ground
68	WL_EN	I	WLAN enable signal. Active high is low in reset.
69	BT_EN	I	Bluetooth enable signal. Active high is low in reset.
70	GND	GND	Ground
71	VDD1V8_AON	PI	1.8 V supply
72	BT_UART_RTS	I/O	UART request-to-send. Active- low request-to-send signal for the HCI UART interface.
73	BT_UART_CTS	I/O	UART clear-to-send Active-low request-to-send signal for the HCI UART interface.
74	BT_UART_TXD	O	UART serial output. Serial data output for the HCI UART interface.
75	BT_UART_RXD	I	UART serial input. Serial data input for the HCI UART interface.
76	LTE_COEX_TXD	O	LTE co-existence signal
77	VDD_PMU	PI	1.8 V supply
78	GND	GND	Ground
79	VDD_CORE_VL	PO	Not Connected (Reserved Point)
80	GND	GND	Ground
81	GND	GND	Ground
82	GND	GND	Ground
83	VDD_PMU	PI	1.8 V supply
84	GND	GND	Ground
85	VDD_CORE_VL	PO	Not Connected (Reserved Point)
86	VDD_CORE_VL	PO	Not Connected (Reserved Point)

87	GND	GND	Ground
88	GND	GND	Ground
89	VDD_CORE_VM	PO	Not Connected (Reserved Point)
90	GND	GND	Ground
91	GND	GND	Ground
92	GND	GND	Ground
93	GND	GND	Ground
94	GND	GND	Ground
95	GND	GND	Ground
96	GND	GND	Ground
97	GND	GND	Ground
98	GND	GND	Ground
99	GND	GND	Ground
100	GND	GND	Ground
101	VDD2P2_1	PI	2.2V supply
102	VDD2P2_1	PI	2.2V supply
103	GND	GND	Ground
104	GND	GND	Ground
105	VDD2P2_2	PI	2.2V supply
106	VDD2P2_2	PI	2.2V supply
107	GND	GND	Ground
108	GND	GND	Ground
109	GND	GND	Ground
110	GND	GND	Ground
111	GND	GND	Ground
112	GND	GND	Ground

3.3 Physical Dimension

3.3.1 Module dimension

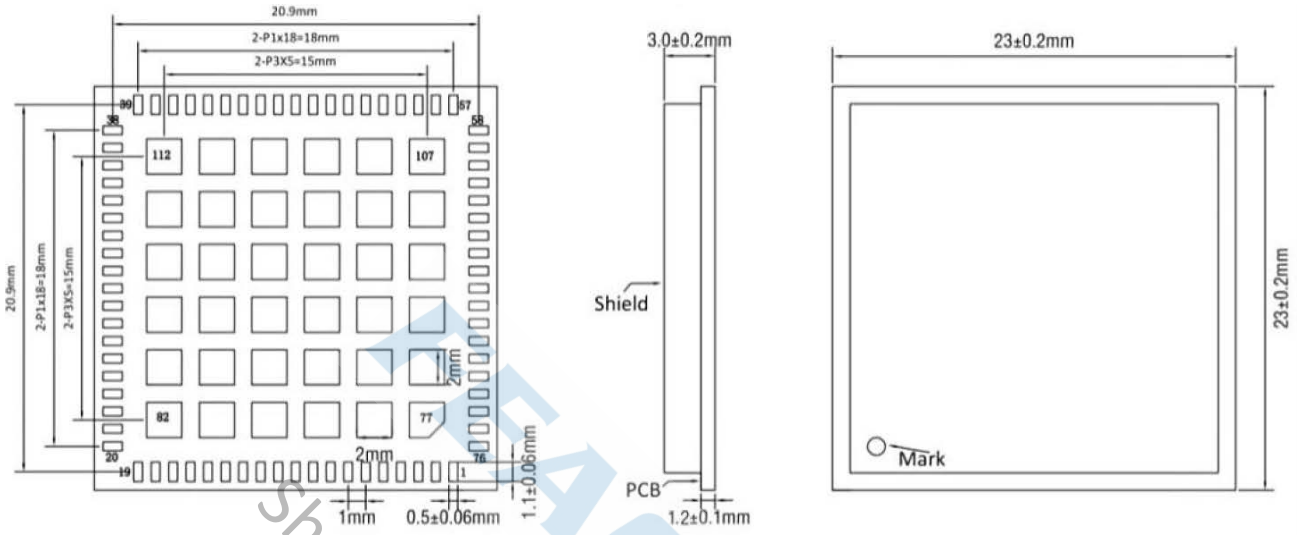


Figure 3-3-1: Module dimension

3.3.2 Recommended Module Mounting Pattern

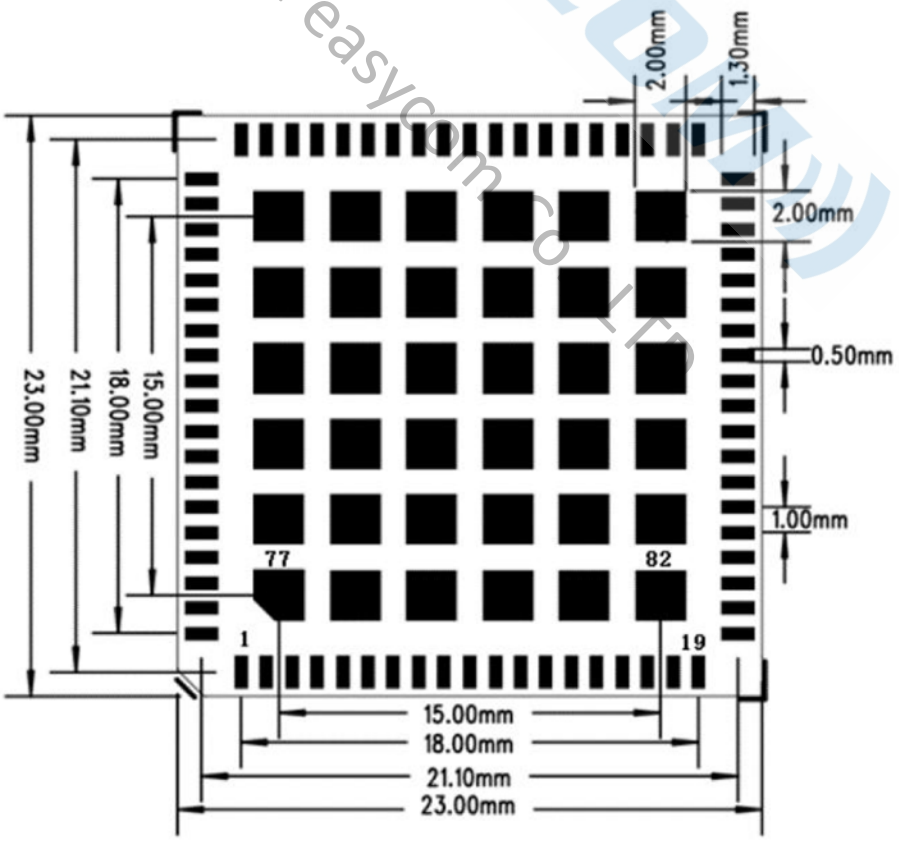


Figure 3-3-2: Recommended Module Mounting Pattern

4 ELECTRICAL CHARACTERISTICS

4.1 Absolute maximum ratings

Table 4-1： Absolute maximum ratings

Parameter	Min	Type	Max	Unit
1.8V power input for PMU	-0.5		1.89	V
2.2V power input for internal PA	-0.5		2.42	V
1.8V power input for Always-On circuits	-0.5		1.89	V
3.3 V supply for VDD_RFSW	0		6.0	V
Maximum Digital I/O Input Voltage	-		2.0	V
Operating temperature range	-40		+85	° C
Storage temperature range	-40		+85	° C
ESD Stress Voltage To be updated after the completion of QUAL (Human Body Model)	-2000		+2000	V

4.2 General Requirements and Operation

Table 4-2： General Requirements and Operation

Parameter	Symbol	Min	Type	Max	Unit
1.8V power input for PMU	VDD_PMU	1.71	1.8	1.89	V
2.2V power input for internal PA	VDD2P2_1	2.09	2.2	2.31	V
1.8V power input for Always-On circuits	VDD1V8_AON	1.71	1.8	1.89	V
3.3 V supply for VDD_RFSW	VDDIO_3V3	3.135	3.3	3.465	V
Input high voltage	V_{IH}	1.4	1.8	1.98	V
Input Low voltage	V_{IL}	-0.3	0	0.3	V
Output high voltage	V_{OH}	1.6	1.8	1.98	V
Output Low voltage	V_{OL}	-0.3	0	0.3	V

5 Module RF Performances

5.1 WLAN Performances

5.1.1 RF Characteristics for IEEE802.11b-2.4G

Table 5-1-1： RF Characteristics for IEEE802.11b-2.4G

Items	Contents
Specification	IEEE802.11b-2.4GHz
Mode	DSSS / CCK
Channel frequency (spacing)	2412 to 2472MHz (5MHz)

Data rate	1, 2, 5.5,11Mbps			
Transmitter	**Min**	**Type**	**Max.**	**Unit**
Power Levels	TBD	-	TBD	dBm
Spectrum Mask				
Spectrum Mask Err	0.0	-	5.12	%
1st side lobes	-	-	-30	dBr
2nd side lobes	-	-	-50	dBr
Center Frequency Tolerance	-20	-	20	ppm
Constellation Error (EVM)	-	-	-10	dB
Receiver	**Min**	**Type**	**Max.**	**Unit**
Minimum Input Level (PER< 8%)	-	-	-76	dBm
Maximum Input Level (PER < 8%)	-10	-	-	dBm

5.1.2 RF Characteristics for IEEE802.11g-2.4G

Table 5-1-2： RF Characteristics for IEEE802.11g-2.4G

Items	**Contents**			
Specification	IEEE802.11g-2.4GHz			
Mode	OFDM			
Channel frequency (spacing)	2412 to 2472MHz (5MHz)			
Data rate	6, 9, 12, 18, 24, 36, 48, 54Mbps			
Transmitter	**Min**	**Type**	**Max.**	**Unit**
Power Levels	TBD	-	TBD	dBm
Spectrum Mask				
Spectrum Mask Err	0.0	-	5.12	%
at fc +/-11MHz	-	-	-20	dBr
at fc +/-20MHz	-	-	-28	dBr
at fc ≧ +/-30MHz	-	-	-40	dBr
Center Frequency Tolerance	-20	-	20	ppm
Constellation Error (EVM)	-	-	-25	dB
Receiver	**Min**	**Type**	**Max.**	**Unit**
Minimum Input Level (PER< 10%)	-	-	-65	dBm
Maximum Input Level (PER < 10%)	-20	-	-	dBm

5.1.3 RF Characteristics for IEEE802.11n(HT20MHz)-2.4G

Table 5-1-3： RF Characteristics for IEEE802.11n(HT20MHz)-2.4G

Items	**Contents**			
Specification	IEEE802.11n-2.4GHz			
Mode	OFDM			
Channel frequency (spacing)	2412 to 2472MHz (5MHz)			
Data rate	6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps			
Transmitter	**Min**	**Type**	**Max.**	**Unit**
Power Levels	TBD	-	TBD	dBm
Spectrum Mask				
Spectrum Mask Err	0.0	--	5.12	%
at fc +/-11MHz	-	-	-20	dBr
at fc +/-20MHz	-	-	-28	dBr
at fc ≧ +/-30MHz	-	-	-45	dBr
Center Frequency Tolerance	-20	-	20	ppm
Constellation Error (EVM)	-	-	-27	dB
Receiver	**Min**	**Type**	**Max.**	**Unit**
Minimum Input Level (PER< 10%)	-	-	-62	dBm
Maximum Input Level (PER < 10%)	-20	-	-	dBm

5.1.4 RF Characteristics for IEEE802.11n(HT40MHz)-2.4G

Table 5-1-4： RF Characteristics for IEEE802.11n(HT40MHz)-2.4G

Items	**Contents**			
Specification	IEEE802.11n-2.4GHz			
Mode	OFDM			
Channel frequency (spacing)	2412 to 2472MHz (5MHz)			
Data rate	13.5,27,40.5,54,81,108,121.5,135Mbps			
Transmitter	**Min**	**Type**	**Max.**	**Unit**
Power Levels	TBD	-	TBD	dBm
Spectrum Mask				
Spectrum Mask Err	0.0	--	5.12	%
at fc +/-11MHz	-	-	-20	dBr
at fc +/-20MHz	-	-	-28	dBr
at fc ≧ +/-30MHz	-	-	-45	dBr
Center Frequency Tolerance	-20	-	20	ppm
Constellation Error (EVM)	-	-	-27	dB
Receiver	**Min**	**Type**	**Max.**	**Unit**

Minimum Input Level (PER< 10%)	-	-	-62	dBm
Maximum Input Level (PER < 10%)	-20	-	-	dBm

5.2 WLAN 11a-5G RF Characteristics

5.2.1 WLAN 11a-5G RF Characteristics for IEEE802.11a-5G

Table 5-2-1： WLAN 11a-5G RF Characteristics for IEEE802.11a-5G

Items	**Contents**			
Specification	IEEE802.11a-5GHz			
Mode	OFDM			
Channel frequency (spacing)	5180 to 5825MHz			
Data rate	6, 9, 12, 18, 24, 36, 48, 54Mbps			
Transmitter	**Min**	**Type**	**Max.**	**Unit**
Power Levels	TBD	-	TBD	dBm
Spectrum Mask				
Spectrum Mask Err	0.0	--	5.12	%
at fc +/-11MHz	-	-	-20	dBr
at fc +/-20MHz	-	-	-28	dBr
at fc ≧ +/-30MHz	-	-	-40	dBr
Center Frequency Tolerance	-20	-	20	ppm
Constellation Error (EVM)	-	-	-25	dB
Receiver	**Min**	**Type**	**Max.**	**Unit**
Minimum Input Level (PER< 10%)	-	-	-65	dBm
Maximum Input Level (PER < 10%)	-30	-	-	dBm

5.2.2 WLAN 11n(HT20MHz)-5G RF Characteristics for IEEE802.11n(HT20MHz)-5G

Table 5-2-2： WLAN 11n(HT20MHz)-5G RF Characteristics for IEEE802.11n(HT20MHz)-5G

Items	**Contents**			
Specification	IEEE802.11n-5GHz			
Mode	OFDM			
Channel frequency (spacing)	5180 to 5825MHz			
Data rate	6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps			
Transmitter	**Min**	**Type**	**Max.**	**Unit**
Power Levels	TBD	-	TBD	dBm

Spectrum Mask				
Spectrum Mask Err	0.0	--	5.12	%
at fc +/-11MHz	-	-	-20	dBr
at fc +/-20MHz	-	-	-28	dBr
at fc ≧ +/-30MHz	-	-	-40	dBr
Center Frequency Tolerance	-20	-	20	ppm
Constellation Error (EVM)	-	-	-27	dB
Receiver	**Min**	**Type**	**Max.**	**Unit**
Minimum Input Level (PER< 10%)	-	-	-62	dBm
Maximum Input Level (PER < 10%)	-30	-	-	dBm

5.2.3 WLAN 11n(HT40MHz)-5G RF Characteristics for IEEE802.11n(HT40MHz)-5G

Table 5-2-3：WLAN 11n(HT40MHz)-5G RF Characteristics for IEEE802.11n(HT40MHz)-5G

Items	**Contents**			
Specification	IEEE802.11n-5GHz			
Mode	OFDM			
Channel frequency (spacing)	5190 to 5795MHz			
Data rate	13.5,27,40.5,54,81,108,121.5,135Mbps			
Transmitter	**Min**	**Type**	**Max.**	**Unit**
Power Levels	TBD	-	TBD	dBm
Spectrum Mask				
Spectrum Mask Err	0.0	--	5.12	%
at fc +/-21MHz	-	-	-20	dBr
at fc +/-40MHz	-	-	-28	dBr
at fc ≧ +/-60MHz	-	-	-40	dBr
Center Frequency Tolerance	-20	-	20	ppm
Constellation Error (EVM)	-	-	-27	dB
Receiver	**Min**	**Type**	**Max.**	**Unit**
Minimum Input Level (PER< 10%)	-	-	-61	dBm
Maximum Input Level (PER < 10%)	-30	-	-	dBm

5.2.4 WLAN 11ac (VHT80MHz)-5G RF Characteristics for IEEE802.11ac(VHT80MHz)-5G

Table 5-2-4：WLAN 11n(HT40MHz)-5G RF Characteristics for IEEE802.11n(HT40MHz)-5G

Items	**Contents**
Specification	IEEE802.11ac-5GHz

Mode	OFDM			
Channel frequency (spacing)	5210 to 5775MHz			
Data rate (MCS0-MCS9)	29.3,58.5,87.8,1 17,175.5,234,263.3,292.5,351,390Mbps			
Transmitter	**Min**	**Type**	**Max.**	**Unit**
Power Levels	TBD	-	TBD	dBm
Spectrum Mask				
Spectrum Mask Err	0.0	--	5.12	%
at fc +/-41MHz	-	-	-20	dBr
at fc +/-80MHz	-	-	-28	dBr
at fc ≧+/-120MHz	-	-	-40	dBr
Center Frequency Tolerance	-20	-	20	ppm
Constellation Error (EVM)	-	-	-32	dB
Receiver	**Min**	**Type**	**Max.**	**Unit**
Minimum Input Level (PER< 10%)	-	-	-51	dBm
Maximum Input Level (PER < 10%)	-30	-	-	dBm

5.3 BT Performance

5.3.1 BT Performance

Table 5-3-1： BT Performance

Parameter	Condition	Std	Unit
Test frequency range	2402 to 2480 MHz		MHz
Step size of Power Control	Channel 0	2～8	dB
	Channel 39		dB
	Channel 78		dB
ICFT (Initial Carrier Frequency Tolerance)	Channel 0	-75～75	KHz
	Channel 39		KHz
	Channel 78		KHz
Output Power	Channel 0	-6～20	dBm
	Channel 39		dBm
	Channel 78		dBm
Carrier Frequency Drift Channel: 0	DH1	25~-25	KHz
	DH1 Drift rata/50us	-20～20	KHz
	DH3	-40～40	KHz
	DH3 Drift rata/50us	-20～20	KHz
	DH5	-40～40	KHz
	DH5 Drift rata/50us	-20～20	KHz

	Channel: 39	DH1	-25～25	KHz
		DH1 Drift rata/50us	-20～20	KHz
		DH3	-40～40	KHz
		DH3 Drift rata/50us	-20～20	KHz
		DH5	-40～40	KHz
		DH5 Drift rata/50us	-20～20	KHz
	Channel: 78	DH1	-25～25	KHz
		DH1 Drift rata/50us	-20～20	KHz
		DH3	-40～40	KHz
		DH3 Drift rata/50us	-20～20	KHz
		DH5	-40～40	KHz
		DH5 Drift rata/50us	-25～25	KHz
Modulation characteristic	Channel: 0	Df1avg	140～175	KHz
		Df2avg	⩾115	KHz
		Df2avg/Df1avg	⩾0.8	
	Channel: 39	Df1avg	140～175	KHz
		Df2avg	⩾115	KHz
		Df2avg/Df1avg	⩾0.8	
	Channel: 78	Df1avg	140～175	KHz
		Df2avg	⩾115	KHz
		Df2avg/Df1avg	⩾0.8	
Sensitivity (single/ multi slot packets) （Power=-70dBm)		Channel 0	BER ⩽ 0.1%	
		Channel 39	BER ⩽ 0.1%	
		Channel 78	BER ⩽ 0.1%	
Maximum input Level （Power=-20dBm)		Channel 0	BER ⩽ 0.1%	
		Channel 39	BER ⩽ 0.1%	
		Channel 78	BER ⩽ 0.1%	

5.3.2 BT EDR Performance

Table 5-3-2： BT EDR Performance

Parameter		Condition	Std	Unit
Test frequency range		2402 to 2480 MHz		MHz
EDR relative power	Channel: 0	PGFSK	－4dB < PDPSK- PGFSK < + 1dB	dB
		PDPSK		dB
	Channel: 39	PGFSK		dB
		PDPSK		dB
	Channel: 78	PGFSK		dB
		PDPSK		dB

EDR carry frequency accuracy and modulation accuracy	Channel: 0 Channel: 39 Channel: 78	RMS DEVM(EDR2) RMS DEVM(EDR3) 99% DEVM(EDR2) 99% DEVM(EDR3) Peak DEVM(EDR2) Peak DEVM(EDR3)	< 0.2 < 0.13 < 0.3 < 0.2 < 0.35 < 0.25
Sensitivity (Power=-70dBm)	Channel: 0 Channel: 39 Channel: 78	EDR2 EDR3	BER≤0.1% BER≤0.1%
Maximum input Level (Power=-20dBm)	Channel: 0 Channel: 39 Channel: 78	EDR2 EDR3	BER≤0.1% BER≤0.1%

5.3.3 BT BLE Performance

Table 5-3-3： BT BLE Performance

Parameter	Condition	Std	Unit
Test frequency range	2402 to 2480 MHz		MHz
ICFT (Initial Carrier Frequency Tolerance)	Channel: 0 Channel: 19 Channel: 39	-100～100	KHz KHz KHz
Output Power	Channel: 0 Channel: 19 Channel: 39	-6～20	dBm dBm dBm
Carrier Frequency Drift	Channel: 0 Channel: 19 Channel: 39	-25~25	KHz KHz KHz
Modulation characteristic	Channel: 0	Df1avg Df2avg Df2avg/Df1avg	225～275 ≥185 ≥0.8	KHz KHz
	Channel:19	Df1avg Df2avg Df2avg/Df1avg	225～275 ≥185 ≥0.8	KHz KHz
	Channel: 39	Df1avg Df2avg Df2avg/Df1avg	225～275 ≥185 ≥0.8	KHz KHz
Sensitivity (Power=-70dBm)	Channel: 0 Channel: 19 Channel: 39	Power=-70dBm Power=-70dBm Power=-70dBm	BER≤0.1% BER≤0.1% BER≤0.1%
Maximum input Level (Power=-20dBm)	Channel: 0 Channel: 19 Channel: 39	Power=-70dBm Power=-70dBm Power=-70dBm	BER≤0.1% BER≤0.1% BER≤0.1%

6 Reliability Test

6.1 Item of Reliability Test

Table 6-1-1： Item of Reliability Test

Test Item	Specification
High Temperature (Storage)	Place 96 hours at 90℃ environment, and 2 hours at normal temperature and humidity then test, module should meet the standard of chapter 6.2.
Low Temperature (Storage)	Place 96 hours at 90℃ environment, and 2 hours at normal temperature and humidity then test, module should meet the standard of chapter 6.2.
High Humidity (Storage)	At the temperature of +60℃, 90%RH environment for 96 hours, and 2 hours at normal temperature and humidity, then test, module should meet the standard of chapter 6.2.
High Temperature (Operating)	At the temperature of +60℃, 90%RH environment for 96 hours, and 2 hours at normal temperature and humidity, then test, module should meet the standard of chapter 6.2.
Low Temperature (Operating)	Module must be able to work continuously for 96 hours at t the environment of -40℃ , The module should work normal within the time or module should meet the standard of chapter 6.2 .
High and low temperature cycling test	Tstg Max 85℃ 30 min s, Temperature shift time: within 2hrs. Tstg Min -40℃ 30 min, Repeat 10 cycles. The module should be cold to normal temperature for two hours, module should meet the standard of chapter 6.2.
Vibration Resistance	Freq: 10~200Hz, 0.1 oct/min, max acceleration: 2.5Grms-Test time: X, Y, Z axis for 6 hours. After 1 hour vibration test, do the test in each direction. In normal temperature condition, take measurements within 3 hours. Module should meet the standard of chapter 6.2.
Shock Test	Shock Test: Impact acceleration: 70G(m/sec2), impact time: 11 mS, impact frequency and direction: 10 times each in 6 directions. In normal temperature condition, take measurements within 3hr， Module should meet the standard of chapter 6.2.
Electrostatic Resistance	Human body model, C=100pF, R=1.5kΩ, ±2kV, INT=0.5S/3times, Take measurements after 2hours in normal condition (Only for shield case and GND).

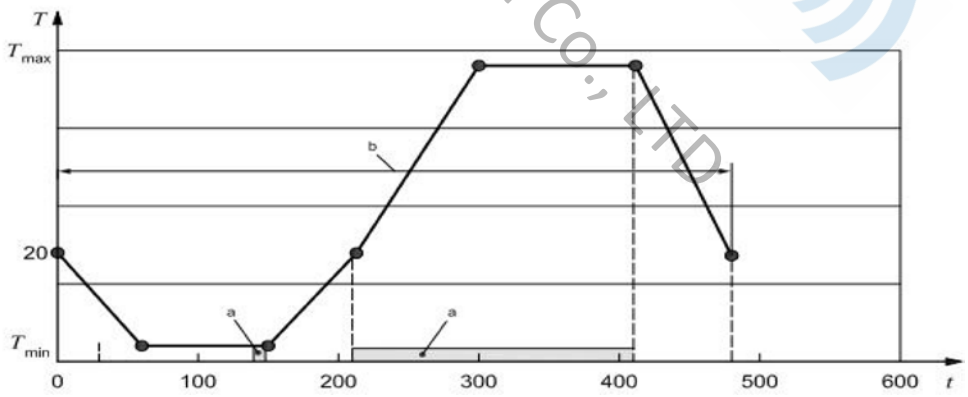


Figure 6-1-1: Temperature cycles with specified change rate

Table 6-1-2： Temperature cycles with specified change rate

Key	
T	temperature, in *C
t	time, in min
T_{min}	minimum operating temperature, in ° C (see Table 1)

T_{max}	maximum operating temperature, in ° C (see Table 1)
a	Operating mode 3.2 in accordance with ISO 16750-1.
b	One cycle

Table 6-1-3：Temperatures and time duration for temperature cycling (see Figure 6-1-1)

Time(min)	Temperature℃
0	20
60	T_{min}
150	T_{min}
2110	20
300	T_{max}
410	T_{max}
480	20
NOTE Codes are in accordance with Table 1 (codes A to T). in the vehicle environment, some equipment might experience different conditions regarding temperatures, temperature gradients and duration: in all these cases, code Z is used。	

6.2 Reliability Test Standard

Table 6-2-1：WLAN 2.4G Performance

Item	Condition	mode	rate	Unit	Std
Transmitter Power	@2412/2437/2462MHz	DSSS CCK	11Mbps 54Mbps	dBm dBm	13~19.5 12~16
EVM	@2412/2437/2462MHz	DSSS	1Mbps 54Mbps	dB dB	≦-10 ≦-25
Receiver sensitivity	At < 10% PER limit @2412/2437/2462MHz	11b mode： DSSS （PER<8%） 11g mode： OFDM （PER<10%）	11Mbps 54Mbps	dBm dBm	≦-82 ≦-65

Table 6-2-2：WLAN 5G Performance

Item	Condition	mode	rate	Unit	Std
Transmitter Power	@5210/5530/5745MHz	11ac OFDM	MCS9	dBm	7~12
EVM	@5210/5530/5745MHz	11ac OFDM	MCS9	dB	≦-32
Receiver sensitivity	@5210/5530/5745MHz	11ac OFDM	MCS9	dBm	≦-51

Table 6-2-3：BT Performance

Parameter	Condition	Std	Unit
Test frequency	2402(Channel0) 2441(Channel39) 2480(Channel78)		MHz
BR Output Power		-6～20	dBm
single/ multi slot packets	Power-70dBm	BER≦ 0.1%	

Sensitivity (Power=-70dBm)

7 PHYSICAL INTERFACE

7.1 Power on and Power off Sequence

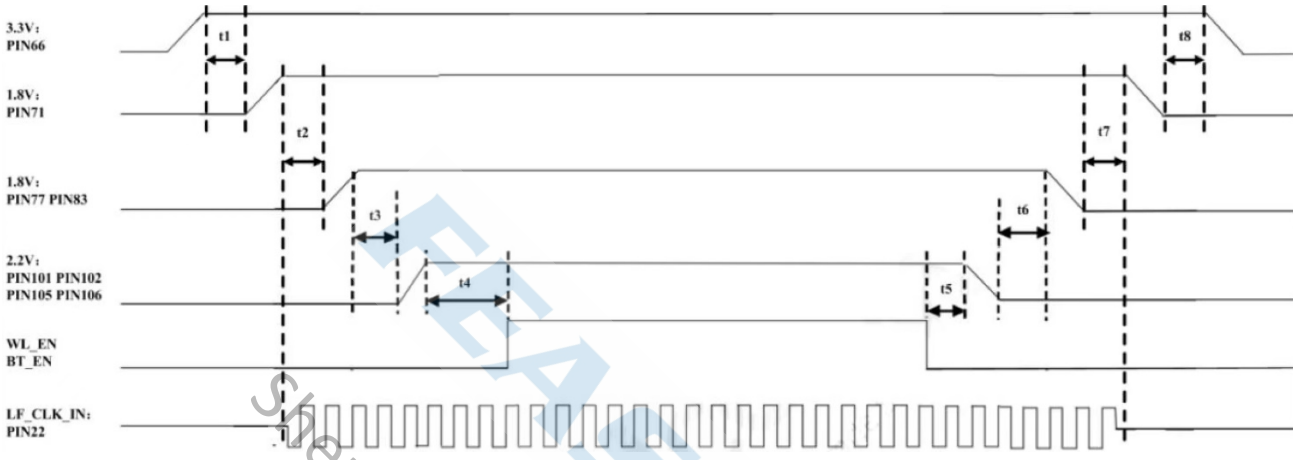


Figure 7-1-1: Power on and Power off Sequence

Table 7-1-1： Power-on timing parameters

Symbol	Description	Min	Max	Units
t1	PIN71 1.8V Start ramping-up	0		us
t2	PIN77 and PIN83 1.8V start ramping-up	10		us
t3	2.2V start ramping-up	0		us
t4	WLAN_EN or BT_EN active	10		us
t5	2.2V start ramping-down 2.2V	10		us
t6	PIN77 and PIN83 1.8V start ramping-down	0		us
t7	PIN71 1.8V start ramping-down	10		us
t8	3.3V start ramping-down	0		us

7.2 PCIE Express Interface

The PCI Express (PCIE) core on the IC is a high-performance serial I/O interconnect that is protocol compliant and electrically compatible with the PCI Express Base Specification v3.0 running at Gen2 speeds. This core contains all the necessary blocks, including logical and electrical functional subblocks to perform PCIE functionality and maintain high-speed links, using existing PCI system configuration software implementations without modification.

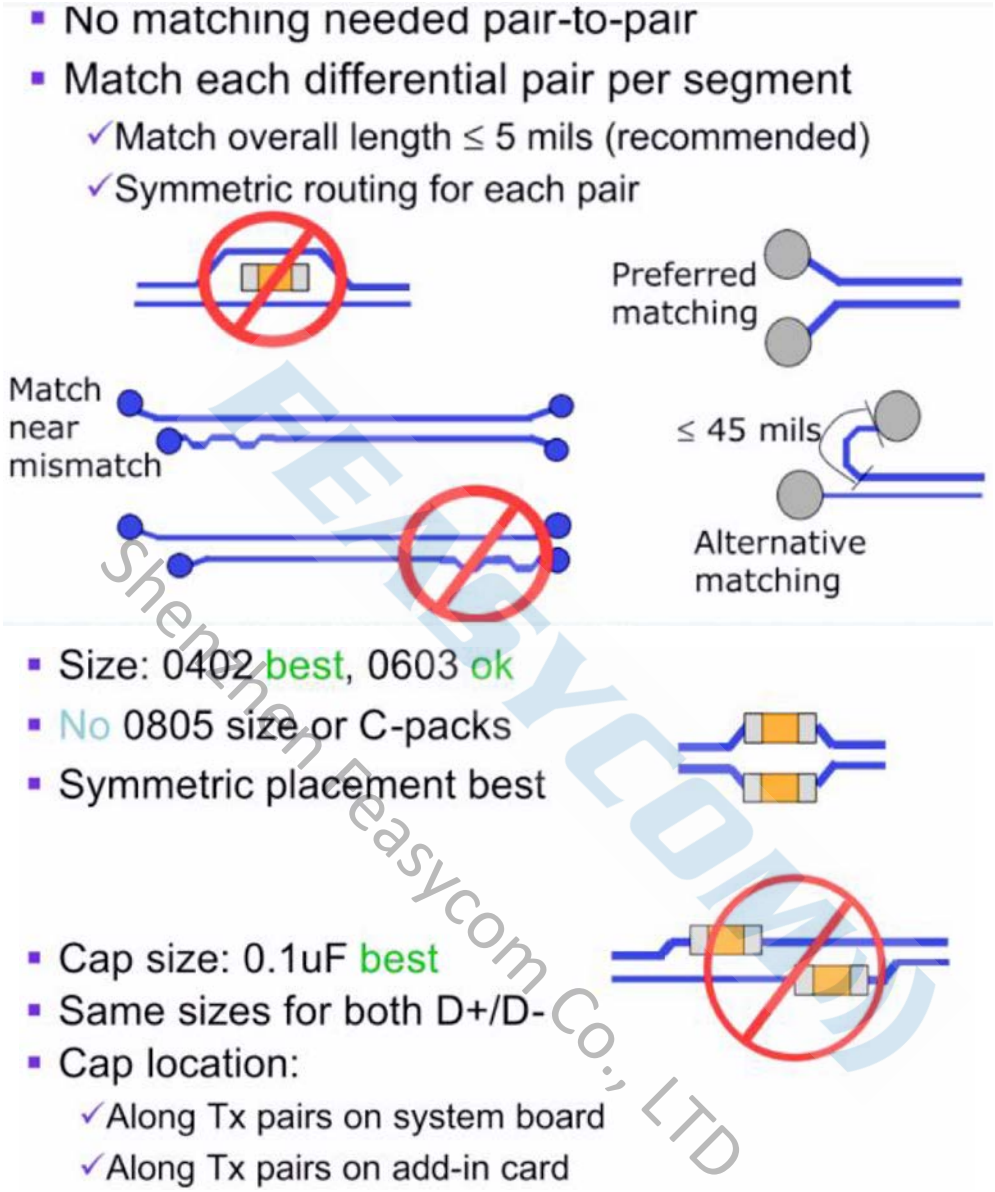
7.3 PCB Layout Recommendation

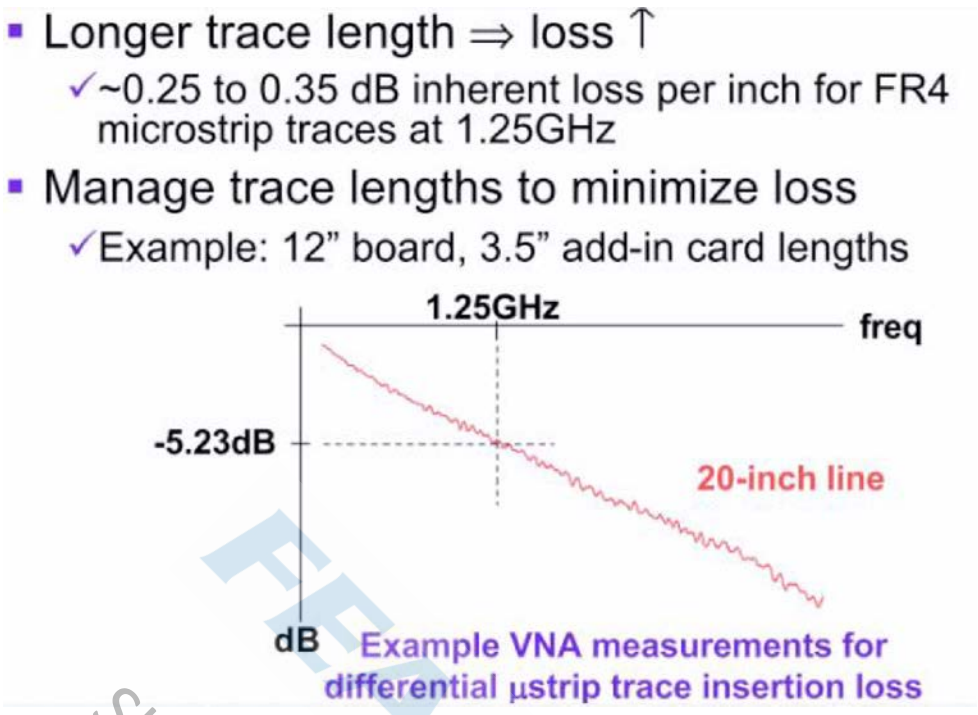
1.PCIE layout guide

The following PCIE routes must comply with the following rules to prevent overshoot/undershoot, because these

routes drive 8mA PCIE_CLK_P & PCIE_CLK_N, PCIE_TX_P & PCIE_TX_N, PCIE_RX_P & PCIE_RX_N.

These pins are differential signals. The path length of these signals is less than 15 CM and the line impedance is less than 100Ω.





2.HCI Lines Layout Guide

The following HCI line routing must comply with the following rules to prevent overshoot or undershoot, because these routes drive 4 to 8 mA.

BT_UART_RTS

BT_UART_CTS

BT_UART_TXD

BT_UART_RXD

The route length of these signals is less than 15 cm. Line impedance less than 50Ω.

3.PCM Lines Layout Guide

The process routing of the following PCM lines must comply with the following rules to prevent overshoot/undershoot as these lines drive 4 mA.

PCM_IN

PCM_OUT

PCM_CLK

PCM_SYNC

The route length of these signals is less than 15 cm. Line impedance less than 50Ω.

7.4 UART Parameters

Table 7-2-1： UART Parameters

Parameter	Value
Number of data bits	Eight

Parity bit	No parity
Stop bit	One stop bit
Flow control	RTS/CTS (hardware)
Flow off response	Two bytes maximum
Supported transport bit rates (bps) [a]	9.6 K, 19.2 K, 38.4 K, 57.6 K, 115.2 K, 125 K, 230.4 K, 250 K, 460.8 K, 500 K, 720 K, 921.6 K, 1 M, 1.6 M, 2 M, 3 M, 3.2 M, with an accuracy of +1.5/-2.5%

[a] UART maximum baud rate is 3.2 Mbps.

- The recommended normal working range of Bluetooth UART Baud rate 115.2～3000 Kbps
- The UART baud rate associated with the use of the system platform, According to the system platform adjust Baud rate.

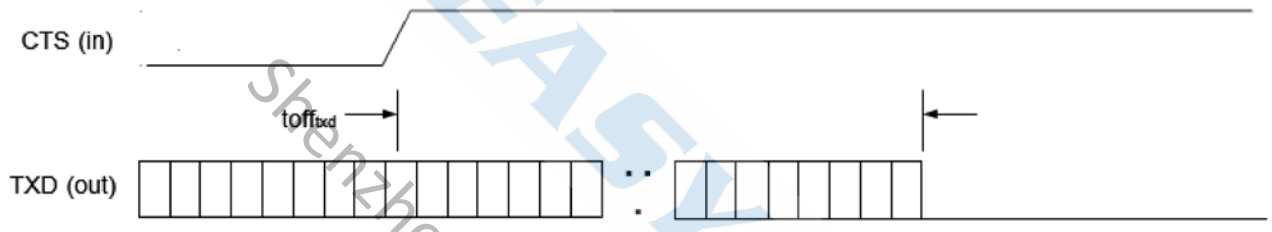


Figure 7-2-1: HCI UART transmit flow control timing

Table 7-2-2： HCI UART transmit flow control timing

Parameter	Description	Min.	Typ.	Max.	Unit
$toff_{txd}$	Delay from CTS to TXD stop			8	byte

The following figure and table show the HCI UART receive timing:

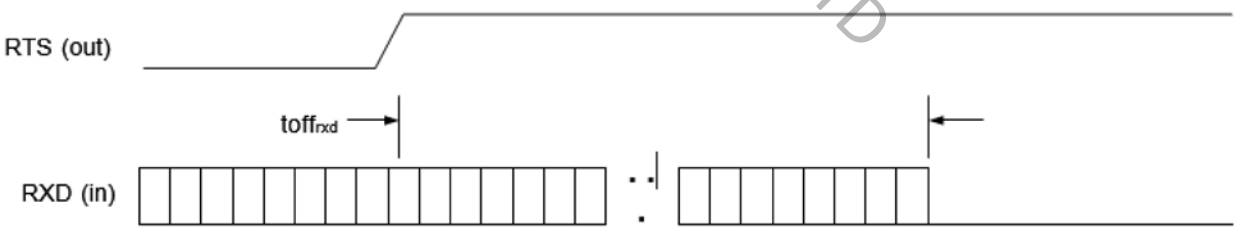


Figure 7-2-2: HCI UART receive flow control timing

Table 7-2-3： HCI UART receive flow control timing

Parameter	Description	Min.	Typ.	Max.	Unit
$toff_{txd}$	Delay from RTS to RXD stop			8	byte

7.5 Bluetooth PCM interface

The pulse coded modulation (PCM) interface connects the QCA6595 device to the phone's audio interface, or to peripheral devices, such as a codec. The PCM interface circuits use digital I/O pins that receive power from the VDD_IO supply.

The QCA6595 PCM interface has been designed to minimize audio latency. The following table lists the typical audio latencies for various packet types:

Table 7-3-1：Typical PCM interface audio latency

Packet type	Audio latency
HV3/EV3 T_{eSCO} = 6, W_{eSCO} = 0	4.4 ms
EV3 T_{eSCO} = 6, W_{eSCO} = 2	5.7 ms
EV3 T_{eSCO} = 6, W_{eSCO} = 4	6.9 ms

The PCM interface is configured to operate as master or slave. In each case, the PCM_IN pin is the data receive terminal (an input), and the PCM_OUT pin is the data transmit terminal (an output). The clock and sync pins function as inputs or outputs, depending on whether the QCA6595 PCM interface is configured as a master or slave:

- When the QCA6595 PCM interface is the master: PCM_CLK and PCM_SYNC are outputs from the QCA6595 to the PCM bus slave(s).
- When the QCA6595 PCM interface is the slave: PCM_CLK and PCM_SYNC are inputs to the QCA6595 device from the PCM bus master.

The following table lists the PCM interface specifications:

Table 7-3-2：PCM interface specifications

Parameter	Description	Min.	Typ.	Max.	Unit
Clock rate (slave)	Determined by the master	64		2,048	kHz
Clock rate (master)	(32 MHz * N/4,000), in which N is an integer, 8 ≤ N ≤ 256	64		2,048	kHz
Frame size		1	8	256	Bits
Slot size		1	13	16	Bits
Slot number	Number of slots that can be configured per frame	1		32	Slots/frame

Example timing diagrams and specifications for slave and master configurations are described in the following figures and tables:

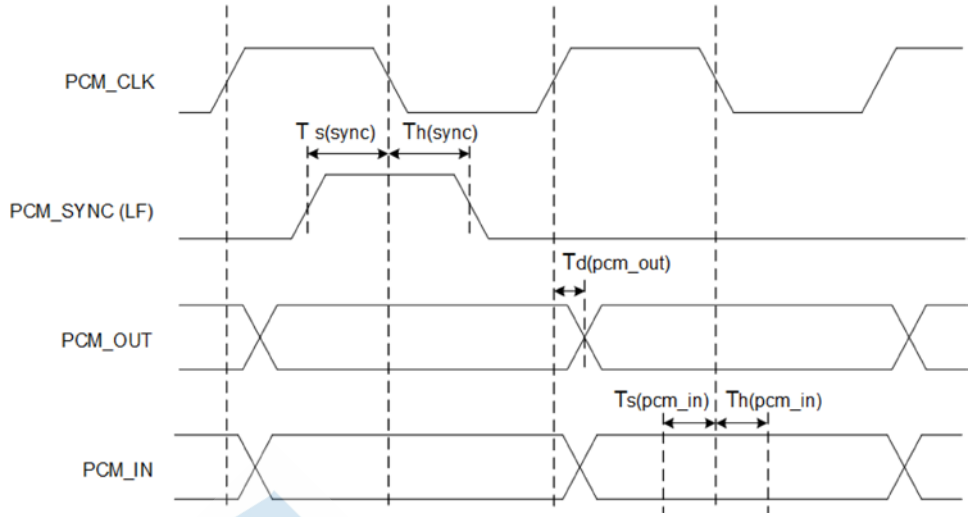


Figure 7-3-1: PCM interface timing diagram (slave)

Table 7-3-3： PCM interface timing in slave mode

Symbol	Description	Min.	Typ.	Max.	Unit
F_{pcm_clk}	PCM_CLK frequency	64		2,048	kHz
Ts_{pcm_sync}	Setup time PCM_SYNC to PCM_CLK fall	0			ns
Th_{pcm_sync}	Hold time PCM_CLK fall to PCM_SYNC fall	150			ns
Td_{pcm_out}	Delay from PCM_CLK rise to PCM_OUT	0		150	ns
Ts_{pcm_in}	Setup time PCM_IN to PCM_CLK fall	0			ns
Th_{pcm_in}	Hold time PCM_IN after PCM_CLK fall	150			ns

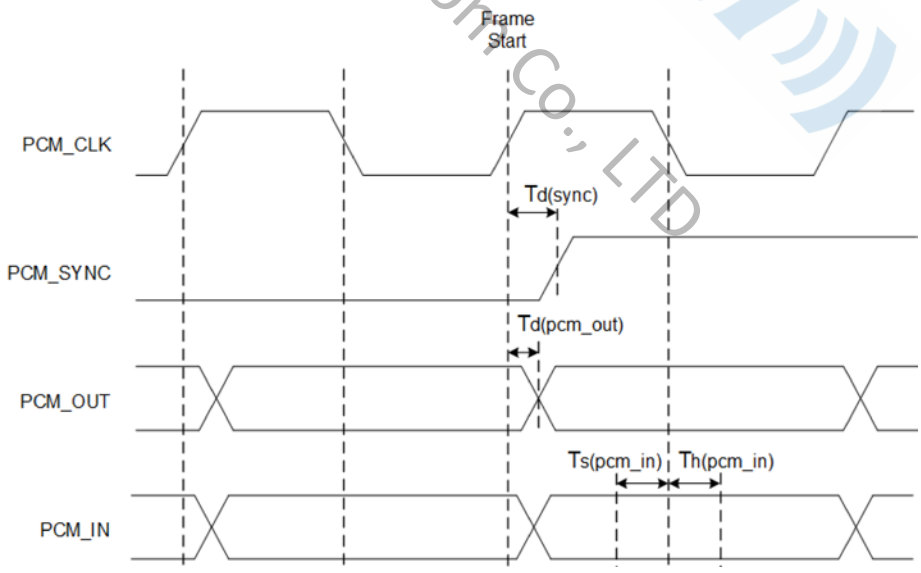


Figure 7-3-2: PCM interface timing diagram (master)

Table 7-3-4： PCM interface timing in slave mode

Symbol	Description	Min.	Typ.	Max.	Unit

F_{pcm_clk}	PCM_CLK frequency	64	2048	kHz
Ts_{pcm_sync}	Delay from PCM_CLK rise to long SYNC	-10	50	ns
Td_{pcm_out}	Delay from PCM_CLK rise to PCM_OUT	-10	50	ns
Ts_{pcm_in}	Setup time PCM_IN to PCM_CLK fall	50		ns
Th_{pcm_in}	Hold time PCM_IN after PCM_CLK fall	150		ns

7.6 I²S timing for slave

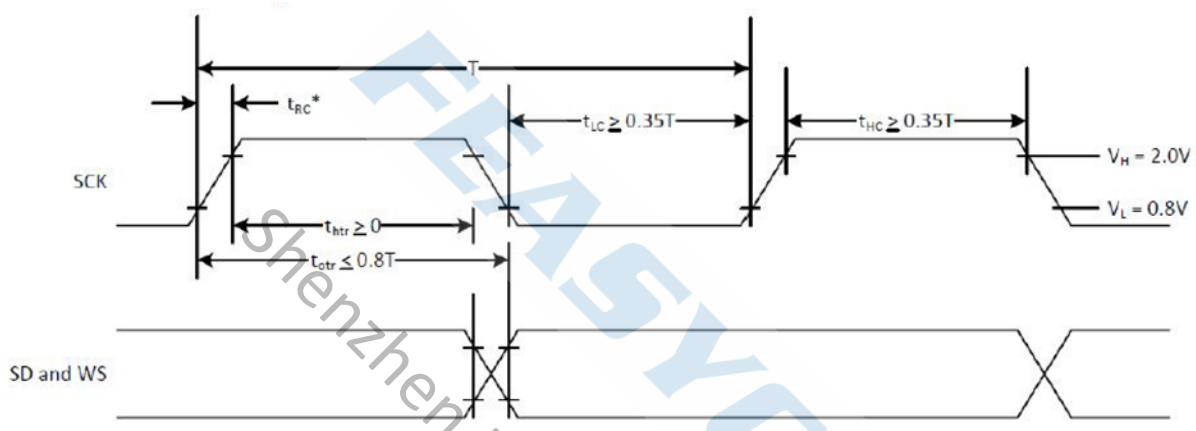


Figure 7-4-1: I²S Transmitters Timing

T= Clock period

T_{tr}= Minimum allowed clock period for transmitter

$T=T_{tr}$

*t_{RC} is only relevant for transmitters in slave mode

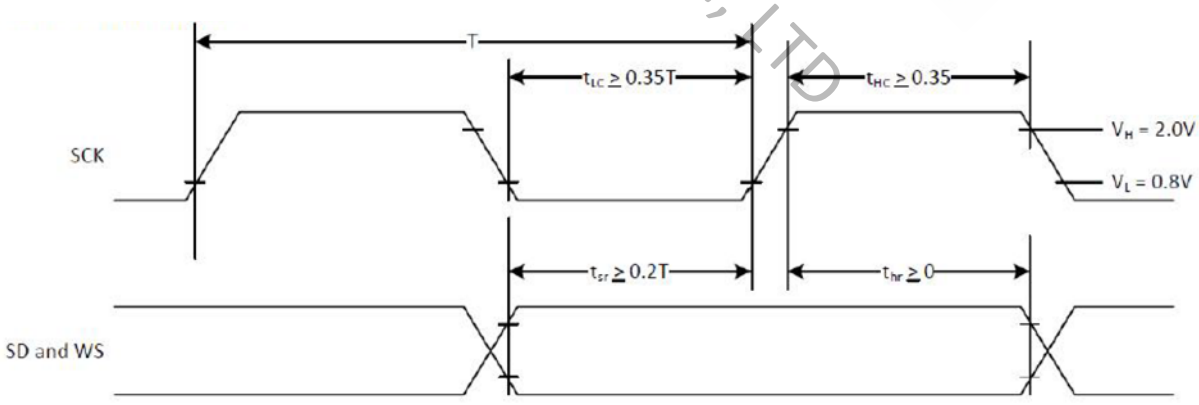


Figure 7-4-2: I²S Receiver Timing

T= Clock period

T_r= Minimum allowed clock period for transmitter

$T>T_r$

Table 7-4-1： Timing for I²S Transmitters and Receivers

	Transmitter				Receiver				
	Lower Limit		Upper Limit		Lower Limit		Upper Limit		
	Min	Max.	Min	Max.	Min	Max.	Min	Max.	Notes
Clock Period T	T_{tr}				T_r				a
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{Hc}	$0.35T_{tr}$				$0.35T_{tr}$				b
LOW_{Lc}	$0.35T_{tr}$				$0.35T_{tr}$				b
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{Hc}		$0.35T_{tr}$				$0.35T_{tr}$			c
LOW_{Lc}		$0.35T_{tr}$				$0.35T_{tr}$			c
Rise time t_{rc}			$0.15T_{tr}$						d
Transmitter									
Delay t_{dtr}				0.8T					e
Hold time t_{htr}		0							d
Receiver									
Setup time t_{sr}						$0.2T_r$			f
Hold time t_{hr}						0			f

7.7 Eternal Digital Slow Clock Requirements (-40 to +85°C)

The following figure and table detail the sleep clock input requirements.

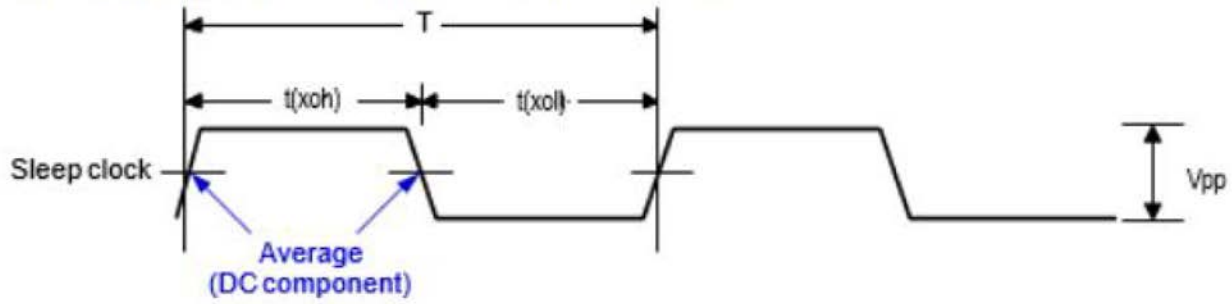


Figure 7-5-1: External sleep clock timing

Table 7-5-1： External sleep clock timing

Parameter	Comments	Min.	Typ.	Max.	Unit

t_{oxh}	Sleep-clock logic high		4.58	25.94	us
t_{xol}	Sleep-clock logic low		4.58	25.94	us
T	Sleep-clock period		30.5208		us
F	Sleep-clock frequency	F = 1T	32.768		kHz
V_{pp}	Peak-to-peak voltage		1.8		V

8 MSL & ESD

Table 8-1: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade	Electrostatic discharge
ESD – Human Body Model (HBM) Rating JESD22-A114-B	Pass ±2000 V, all pins
ESD – Charged Device Model (CDM) Rating JESD22-C101-D	Pass ±250 V, all pins

9 RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Notice (注意) :

Feasycom module must use Step-Stencil, suggestion using the stencil thickness about 0.16-0.2mm, it could be modify with the product.

使用我司模块，须使用阶梯钢网，建议阶梯钢网厚度0.16-0.20mm，可根据自己产品适应性，进行相应调整.

Table 9-1: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%

3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

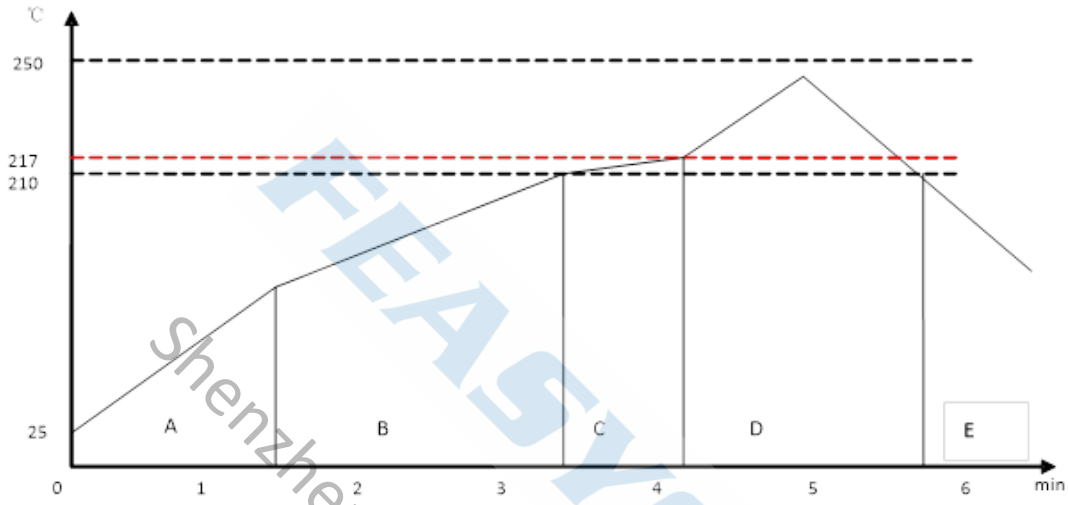


Figure 9-1：Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

10 MECHANICAL DETAILS

10.1 Mechanical Details

- Dimension: 23mm(W) x 23mm(L) x 2.9mm(H) Tolerance: ±0.2mm
- Module size: 23mm X 23mm Tolerance: ±0.2mm
- Pad size: 1.3mmX0.5mm Tolerance: ±0.1mm
- Pad pitch: 1.0mm Tolerance: ±0.1mm

(分板后边角残留板边误差：不大于 0.5mm) (Residual plate edge error: < 0.5mm)

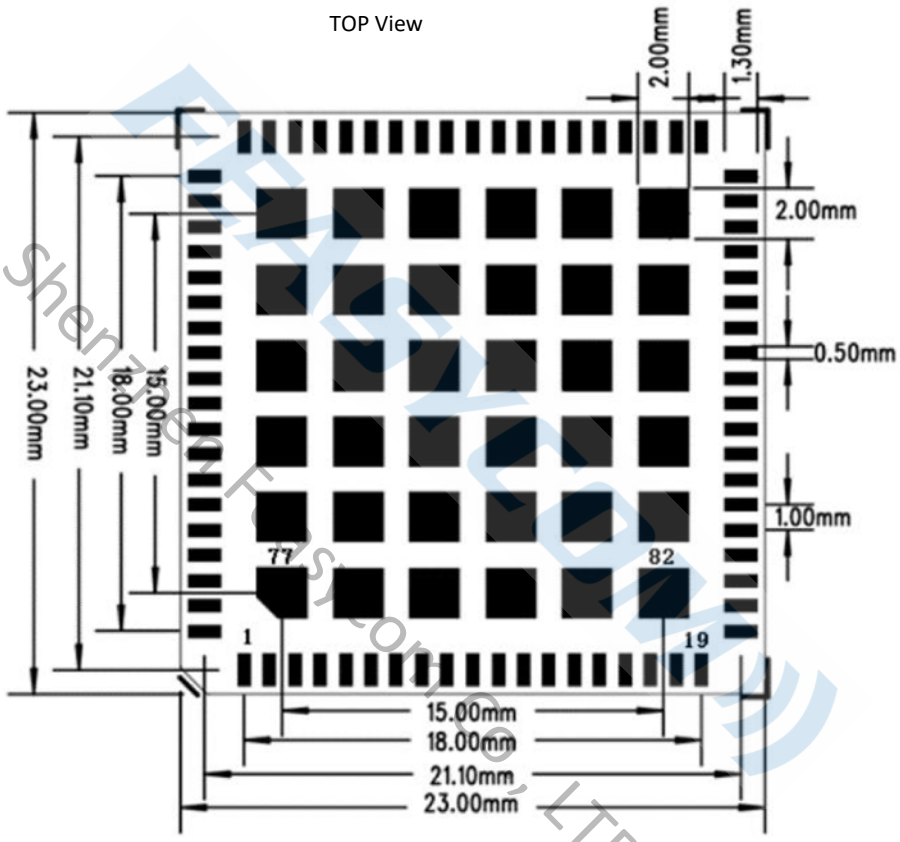


Figure 10-1： FSC-BW3051 footprint Layout Guide (Top View)

11 HARDWARE INTEGRATION SUGGESTIONS

11.1 Requirement for the 3.3V power supply

- To use a dedicated power supply circuit for Wi-Fi (and BT).
- <0.05% line regulation and <0.5%/A load regulation are required for ripple frequency below 100KHz.
- Transient-response: 1, The ripple raised from 100/800mA step-response test should be small than 200mVpp. 2, The ripple swing shall settle down within 1~2 cycles, 2 cycles for the worst case.

- Power supply spur: make sure the spurs from switching mode power supply or other noisy circuits are reasonably small. Once issue concerned with such a power supply spur, alternative power supply filtering might be needed.
- VDD_3V3: 3.0 to 3.6V (Peak Current 1.5A); VDD_IO: 1.7 to 3.6V (Peak Current 200mA)

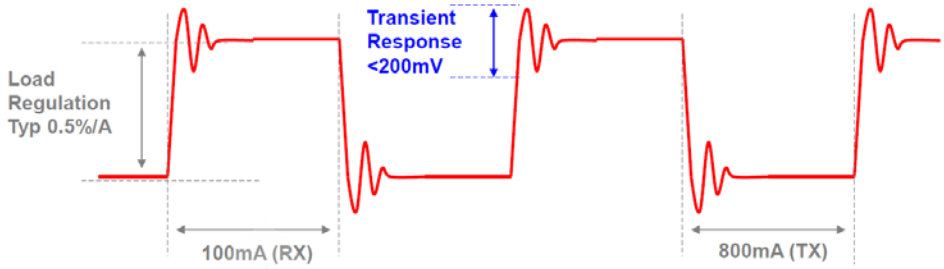


Figure 11-1: Requirement for the 3.3V power supply

11.2 Connections when BT's HCI is by UART

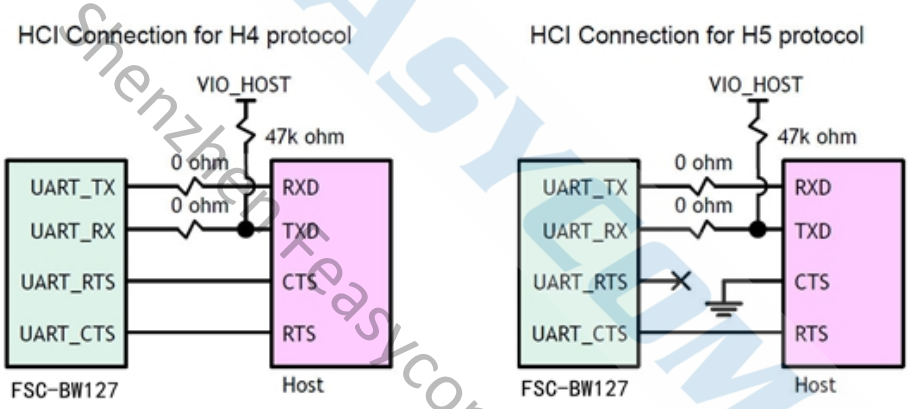


Figure 11-2: Connections when BT's HCI is by UART

Note:

1. Reserve a 47k pull-high resistor on host TXD when this port is not in output mode for default.

   (If not sure, reserve a 47k resistor is recommended for avoid TXD being floating)

2. There must be 0 ohm jumper-resistors on TX/RX paths, for BQB certification test.

11.3 RF Circuit- RF pads

- Some RF components such as 0402-packaged RLC, connectors, or module pins are with large soldering pad, those pads have higher parasitic capacitance which can impact the characteristic impedance of RF traces.
- The GND under those pads shall be dug out, shown as below, for keeping good 50Ω matching.
- The dig-out layers and area should be calculated carefully, we recommend digging the area a little higher than the simulation results.

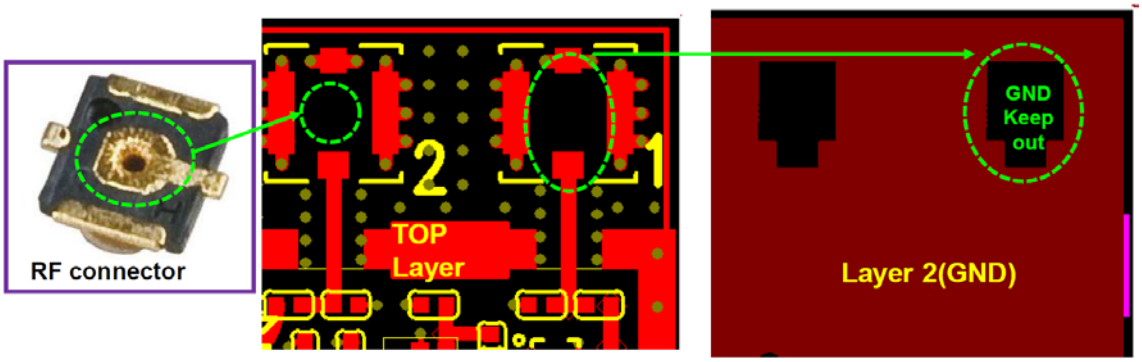


Figure 11-3: RF Circuit- RF pads

11.4 Recommendable antenna & IPEX by Feasycom

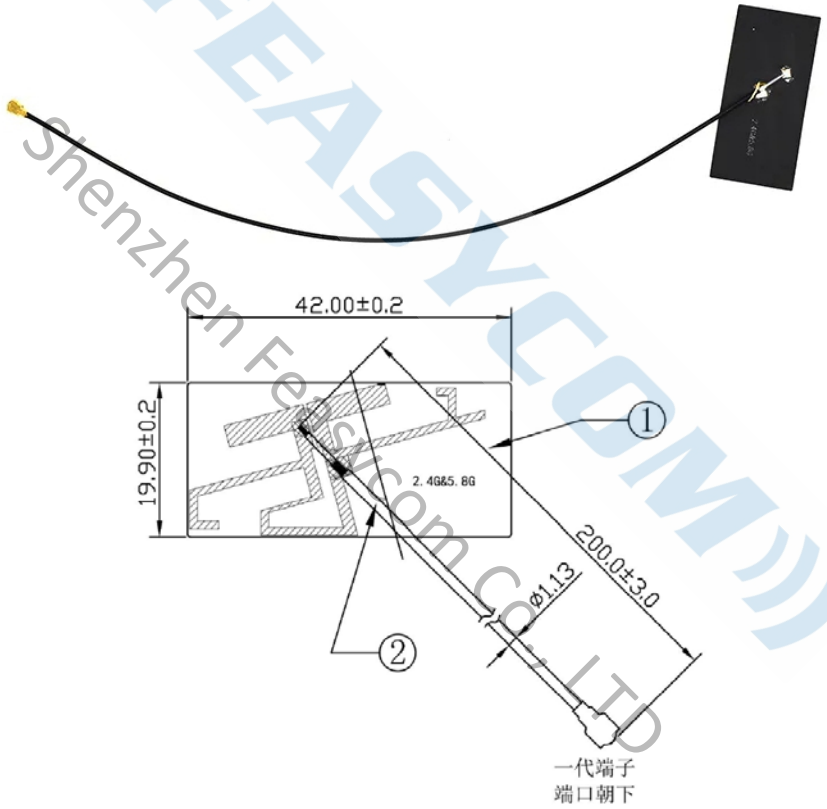
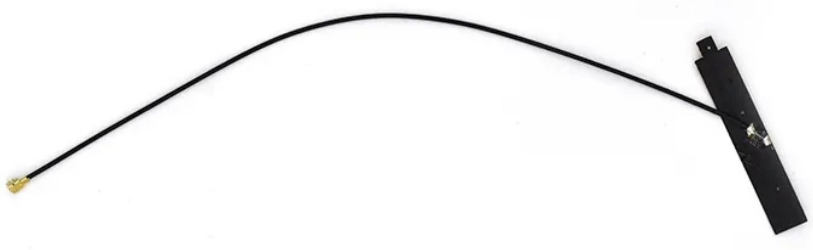


Figure 11-4-1: 2.4GHz & 5GHz Dual-band antenna, with IPEX first generation interface



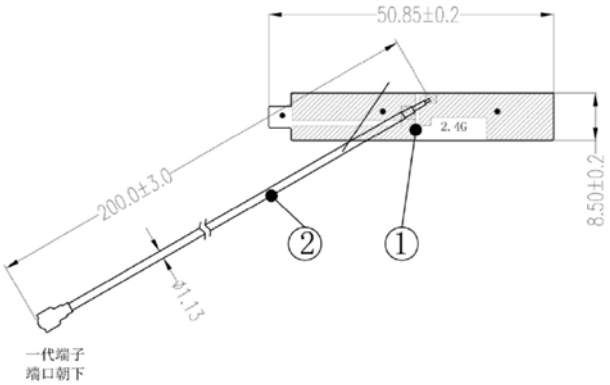
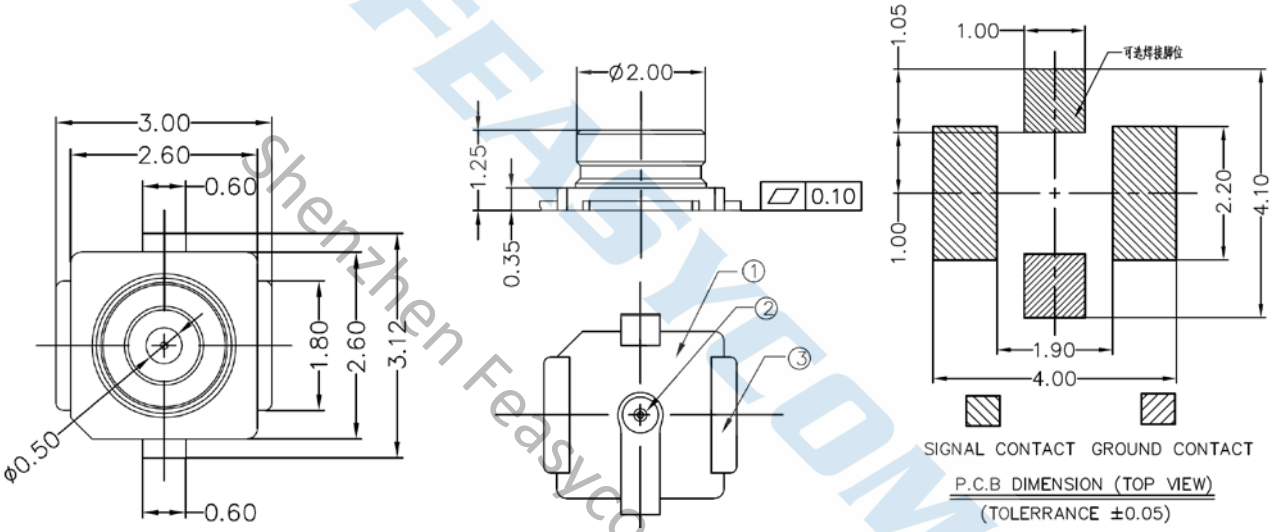


Figure 11-4-2: 2.4GHz antenna with IPEX first generation interface



ITEM	NAME	Q'TY	MATERIAL ⚠1	FINISH ⚠2
3	GROUND CONTACT	1	JIS C5191-H	Au 1u" Min. over Ni 50~100u" Min.
2	CONTACT	1	JIS C2680-1/4H	Au 1u" Min. over Ni 50~100u" Min.
1	HOUSING	1	LCP E6808	UL94V-0,30% GF

NOTES:
1. FREQUENCY RANGE:
   DC TO 6GHZ (VSWR: 1.3MAX AT 0.1~3GHZ, 1.4MAX AT 3~6GHZ)
2. CHARACTERISTIC IMPEDANCE: 50 (NOMINAL);
3. TEMPERATURE: −40°C TO +90°C;
4. RATED VOLTAGE : 60VAC;
5. CONTACT RESISTANCE :
   20m MAX.(SIGNAL CONTACT)
   20m MAX.(GROUND CONTACT)
6. WITHSTAND VOLTAGE : 200VAC FOR 1 MINUTE MIN;
7. INSULATION RESISTANCE : 500M MIN. AT 100VDC;
8. THIS COMPONENT IS HALOGEN FREE.

Figure 11-4-3: IPEX first generation interface

11.5 Soldering Recommendations

FSC-BW3051 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum

profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

11.6 Layout Guidelines (Internal Antenna)

Important Note: The antenna for FSC-BW3051 is suggested to support both 2.4GHz and 5.8GHz dual frequency bands. We recommend using external FPC dual-band antennas instead of PCB onboard antennas. The following are general instructions for PCB onboard antennas for reference only.

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

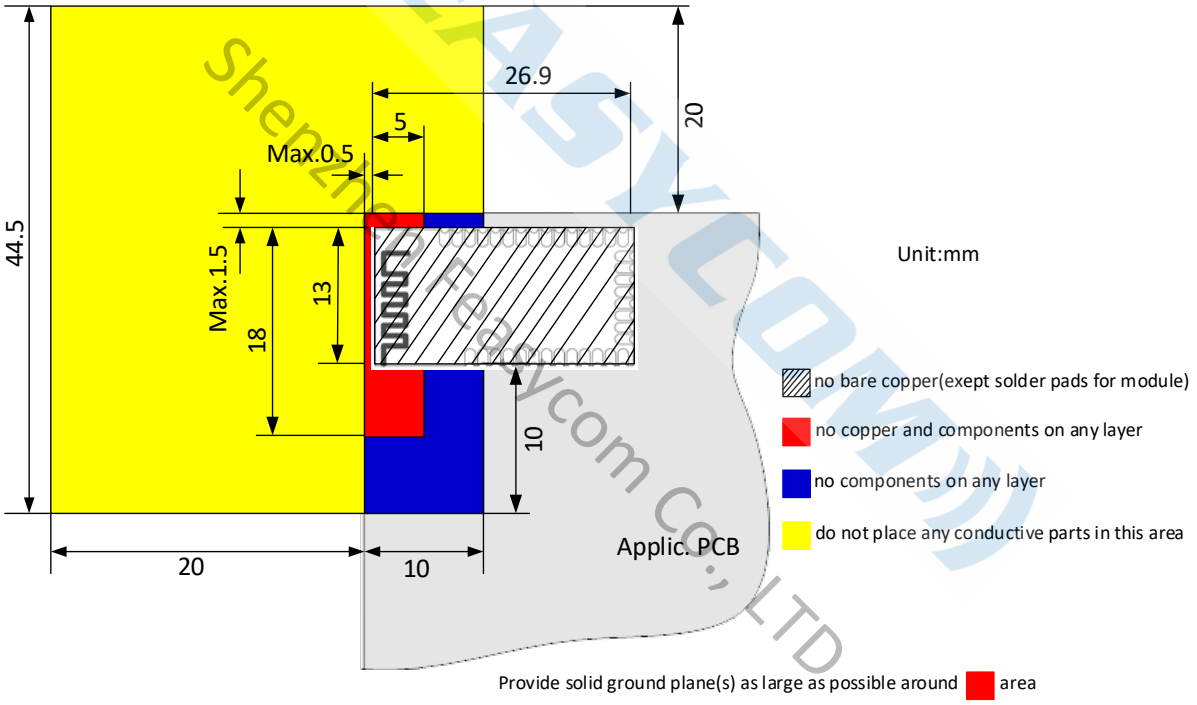


Figure 11-6： Restricted Area (Design schematic, for reference only. Unit: mm)

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

11.7 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

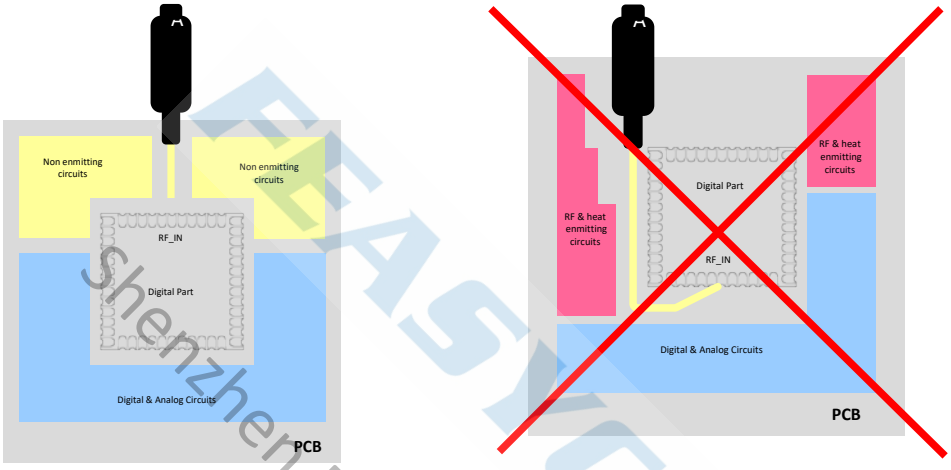


Figure 11-7: Placement the Module on a System Board

11.7.1 Antenna Connection and Grounding Plane Design

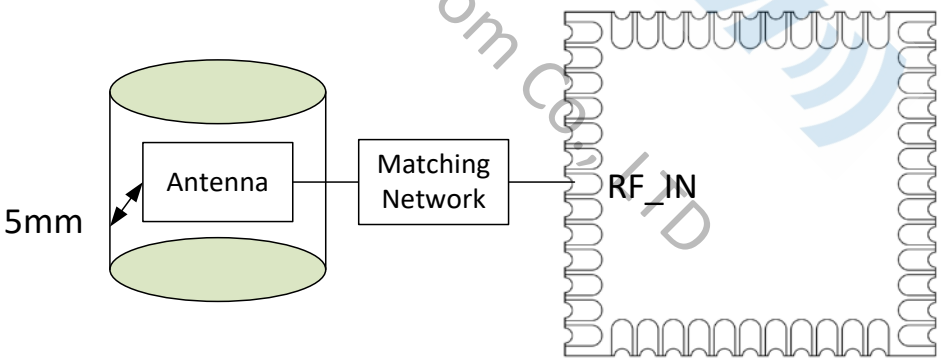


Figure 11-7-1: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.

➢ To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

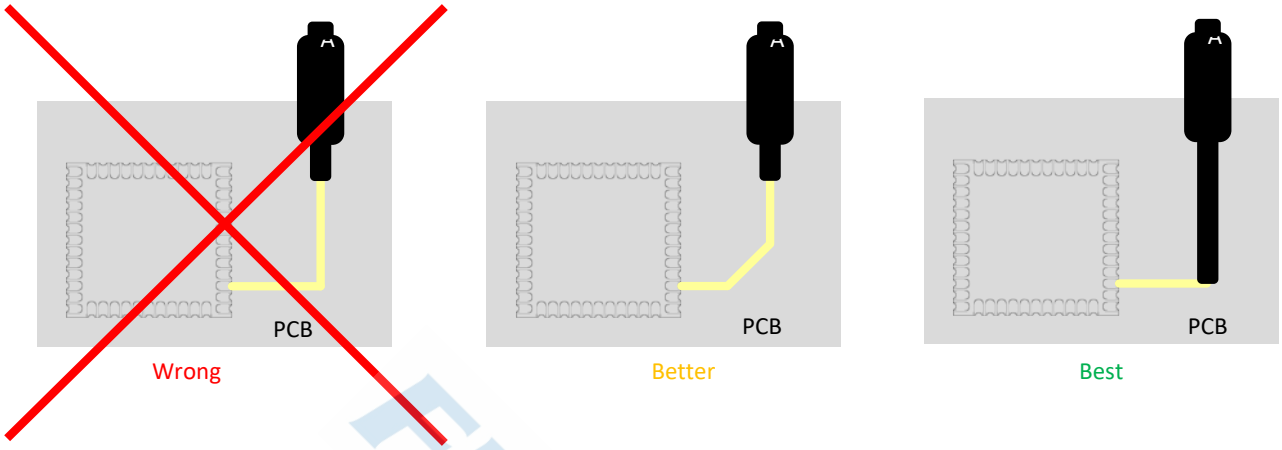


Figure 11-7-2: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

11.8 SDIO Lines Layout Guideline

The following SDIO line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 8mA.

SDIO_CMD

SDIO_CLK

SDIO_D0 ~ SDIO_D3

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω

11.9 HCI Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 ~ 8mA

UART_RX

UART_TX

UART_CTS

UART_RTS

The route length of these signals be less than 15cm and the line impedance be less than 50Ω

11.10 Power Trace Lines Layout Guideline

VDD_3V3 Trace Width: 40mil

VDD_IO Trace Width: 20mil

11.11 Ground Lines Layout Guideline

A Complete Ground in Ground Layer.

Add Ground Through Holes to FSC-BW3051 Module Ground Pads

Decoupling Capacitors close to FSC-BW3051 Module Power and Ground Pads

12 PRODUCT PACKAGING INFORMATION

12.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 160mm * 310mm

Figure 12-1: Tray vacuum

12.2 Packing box (Optional)

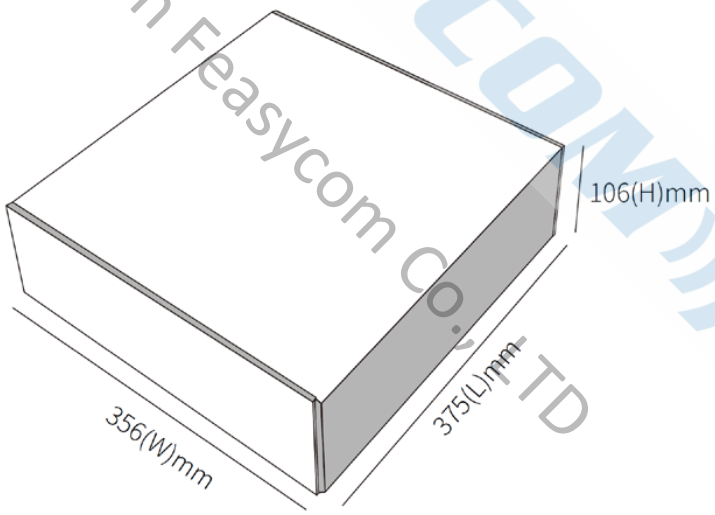


Figure 12-2: Packing box(Optional)

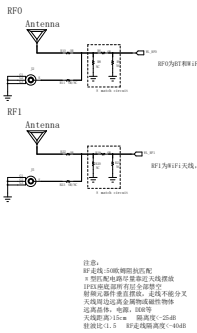
** If other packing is required, please confirm with the customer*

** Packing: 1000pcs per carton (Minimum packing quantity)*

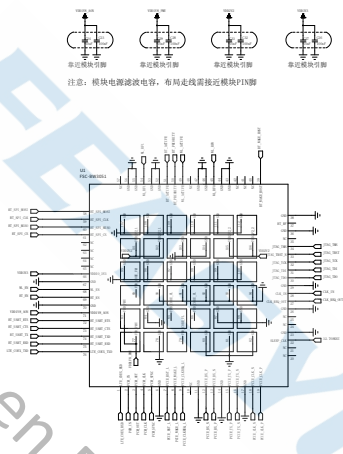
** The outer packing size is for reference only, please refer to the actual size*

13 APPLICATION SCHEMATIC

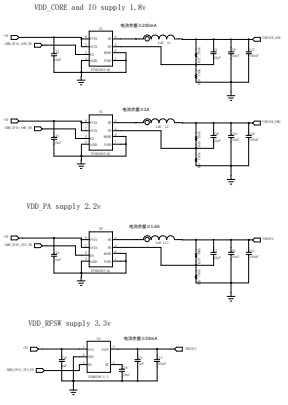
RF



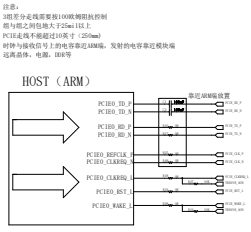
模组



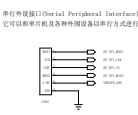
电源



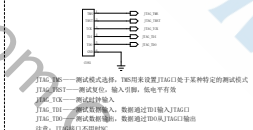
PCIE接口



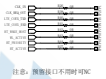
SPI调试接口



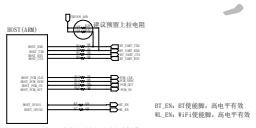
JTAG调试接口



预留接口



串口、PCM、WL_EN和BT_EN



外部低功耗32.768 kHz时钟