FSC-BW1501UV

DATASHEET V1.1

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Revision History

Version	Data	Notes	Author
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V1.1	2024-12-05	Update parameter	Liu

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1 INTRODUCTION

Overview

BW1501UV is a highly integrated single chip which features a low power 2x2 802.1 1a/b/g/n/ac/ax dual-band Wi-Fi subsystem and a Bluetooth v5.4 subsystem, offering feature-rich wireless connectivity at high standards, and delivering reliable, cost-effective throughput from an extended distance.

Optimized RF architecture and baseband algorithms provide superb performance and low power consumption. Intelligent MAC design deploys a high efficient offload engine and hardware data processing accelerators which fully offloads Wi-Fi task of the host processor. BW1501UV is designed to support standard based features in the areas of security, quality of service and international regulations giving end users the greatest performance any time and in any circumstance.

BW1501UV is designed to support high data throughput over Wi-Fi. The host interface PCle2.1 is integrated to provide stable bandwidth between the host platform and BW1501UV. The clock rate of the internal bus fabric can also support the throughput the requirement. The clock rate of MCU is also configurable for different kinds of scenarios.

BW1501UV supports low power requirement. Multiple power domains are implemented on chip. It defines a deep sleep mode, in which only the AON domain is powered on, while other OFF domains are shut off by the power switches integrated on chip. In deep sleep mode, the PMU could be further configured to be in a low power state to save the power consumption.

BW1501UV has the Wi-Fi MAC, BBP, and the RF subsystems, which provide the best-in-class radio and low power performance, coexistence of 4G.

BW1501UV has the Bluetooth LC/BB and the RF subsystems.

General Features

- 32-bit RISC MCU for Wi-Fi/Bluetooth protocols and Wi-Fi offload.
- BT & Wi-Fi 2.4GHz built in BAW filter.
- Embedded SRAM/ROM.
- USB interface with hardware flow control.
- Programmable and multiplexed GPIO pins.
- PCIe device fully compliant to PCIe v2.1 specification.
- Advanced FDD/TDD mode Wi-Fi/Bluetooth coexistence scheme.
- Integrate 20Kbit efuse to store devices specific information and RF calibration data.

WLAN Features

- IEEE 802.11 a/b/g/n/ac/ax compliant.
- Support 20MHz, 40MHz, 80Mhz bandwidth in 2.4GHz, 5GHz, 6GHz band.
- Dual-band 2T2R mode.
- Support MU-MIMO RX.
- Support uplink MU-OFDMA TX and downlink MU-OFDMA RX.
- Support DBDC (dual band dual concurrent).

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- Support STBC, LDPC, TX Beamformer and RX Beamformer
- Greenfield, mixed mode, legacy modes support.
- IEEE 802.11 d/e/h/i/j/k/mc/r/v/w support.
- Security support for WFA WPA/WPA2/WPA3 personal. WPS2.0.
- QoS support of WFA WMM, WMM PS.
- Integrated LNA, PA, and T/R switch.
- Optional external LNA and PA support.
- Interface: PCIE2.1 Data rate up to 1024Mbps.

Bluetooth Features

- Bluetooth v5.4 with BLE (BT low energy).
- Supports BT/BLE dual mode.
- Supports BT/Wi-Fi coexistence.
- Supports 7 BT links and 16 BLE link.
- Supports SCO and eSCO link with re-transmission.
- Supports wide-band speech.
- Supports mSBC and SBC including mono and stereo.
- Supports Packet Loss Concealment (PLC) function for better voice quality.
- Supports LE Isochronous channels.
- Supports LC3 including mono and stereo.
- Supports secure connection with AES128 and ECC256.
- Channel quality driven data rate adaptation.
- Channel assessment and WB RSSI for AFH.

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2 General Specifications

Table 2-1: General Specifications

Categories	Features	Implementation
Chip type		MT7921AEN
Bluetooth		
	Bluetooth Standard	Support Bluetooth 5.4+EDR
	Frequency Band	2.402G ~ 2.480G
	Interface	UART, PCM/I2S
	RF Input Impedance	50 ohms
WLAN		
	Frequency Band	2.4GHz/5GHz/6GHz
	RF Input Impedance	50 ohms
	Interfaces	PCIE
operate condition		
	VDDIO	1.8V
	VDD_3V3	3.3V
	Operating Temperature	-40°C to +85°C
	Storage temperature	-40°C to +85°C
	Humidity	10%~90% Non-Condensing
Dimension		
	Dimension	23mm(L)*23mm(W)*3.0mm(H)
	coplanarity	<=0.1mm (ordinary temperature 25°C
	ROHS	ROHS2.0

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3 HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

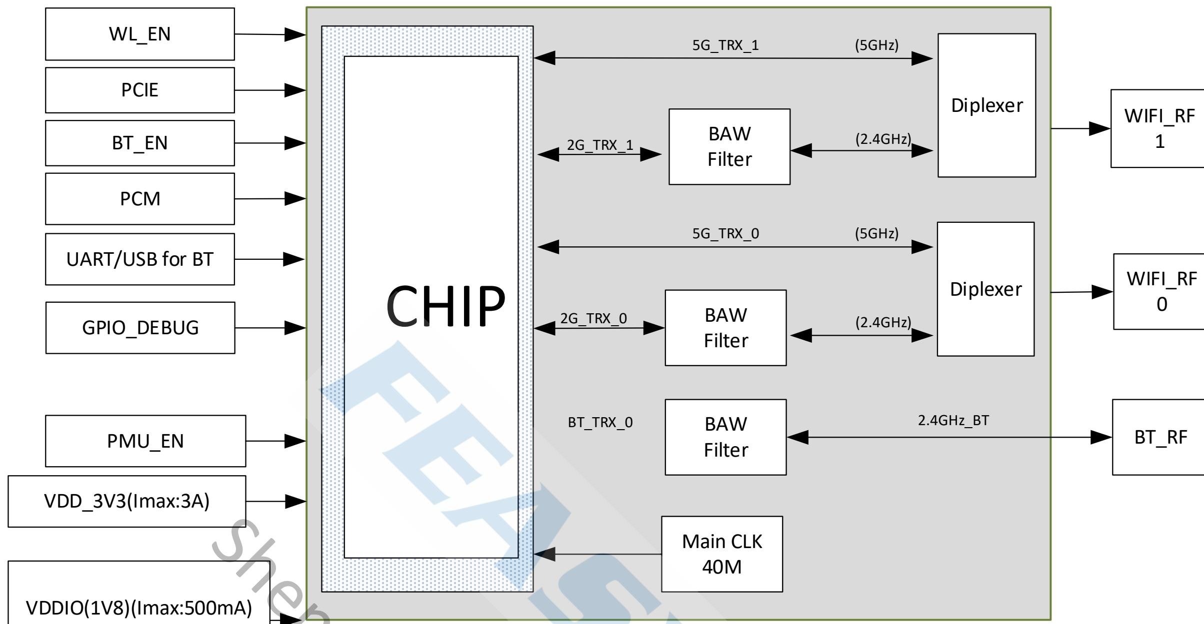

Figure 3-1-1: FSC-BW1501UV Block Diagram

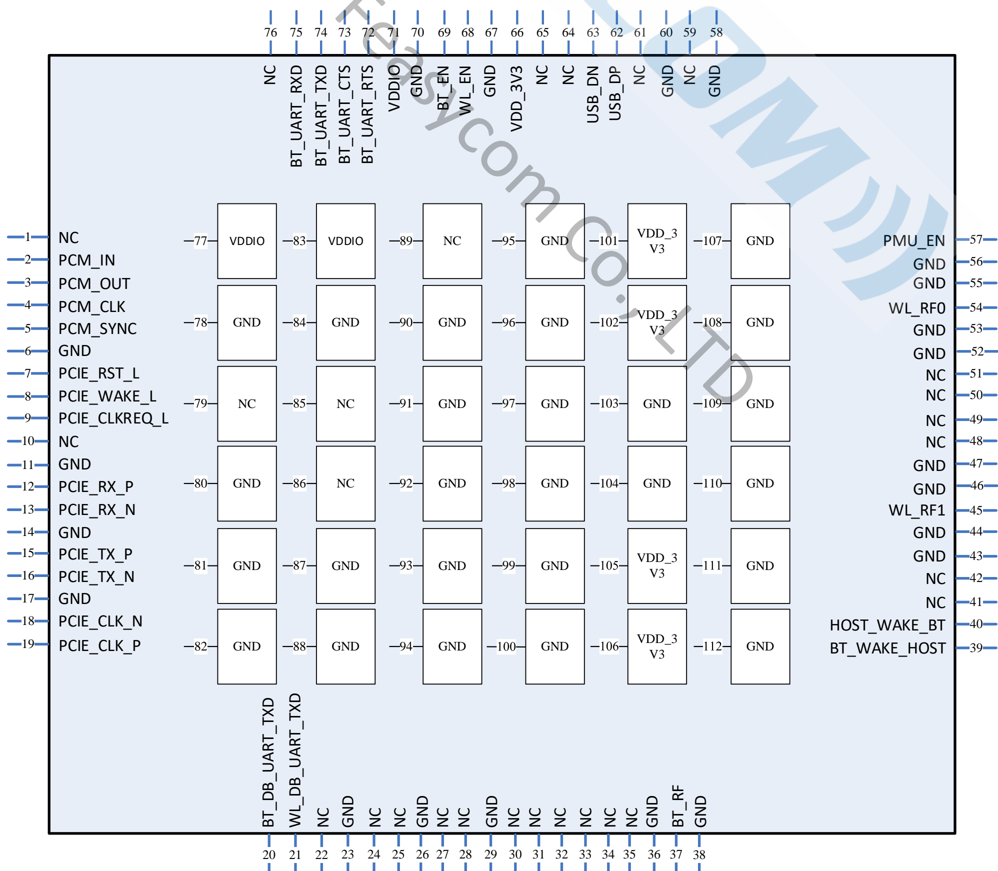

Figure 3-1-2: FSC-BW1501UV PIN Diagram (Top View)

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3.2 PIN Definition Descriptions

Table 3-2： Pin definitions

Pin	Pin Name	Type	Pin Descriptions	Notes
1	NC	NC	Not Connected	
2	PCM_IN	I	BT PCM/I2S Bus Data in	
3	PCM_OUT	O	BT PCM/I2S Bus Data out	
4	PCM_CLK	I	BT PCM/I2S Bus Clock in	
5	PCM_SYNC	I	BT PCM/I2S Bus Frame sync BT	
6	GND	GND	Ground	
7	PCIE_RST_L	I	PCI express reset with weak pull-down	
8	PCIE_WAKE_L	O	Request to service a function -initiated Wake Event. (an external pull-up resistor to 1.8V is required)	
9	PCIE_CLKREQ_L	O	Reference clock request	
10	NC	NC	Not Connected	
11	GND	GND	Ground	
12	PCIE_RX_P	I	PCI Express Receive Differential Pair	
13	PCIE_RX_N	I		
14	GND	GND	Ground	
15	PCIE_TX_P	O	PCI Express Transmit Differential Pair	
16	PCIE_TX_N	O		
17	GND	GND	Ground	
18	PCIE_CLK_N	I	PCI Express Differential Reference.	
19	PCIE_CLK_P	I		
20	BT_DB_UART_TXD	O	GPIO For DEBUG	
21	WL_DB_UART_ TXD	O	GPIO For DEBUG	
22	NC	NC	Not Connected	
23	GND	GND	Ground	
24	NC	NC	Not Connected	
25	NC	NC	Not Connected	
26	GND	GND	Ground	
27	NC	NC	Not Connected	
28	NC	NC	Not Connected	
29	GND	GND	Ground	
30	NC	NC	Not Connected	
31	NC	NC	Not Connected	
32	NC	NC	Not Connected	
33	NC	NC	Not Connected	
34	NC	NC	Not Connected	
35	NC	NC	Not Connected	
36	GND	GND	Ground	

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37	BT_RF	RF	Not Connected
38	GND	GND	Ground
39	BT_WAKE_HOST	O	Bluetooth wake up the host
40	HOST_WAKE_BT	I	host wake up the Bluetooth
41	NC	NC	Not Connected
42	NC	NC	Not Connected
43	GND	GND	Ground
44	GND	GND	Ground
45	WL_RF1	RF	WIFI 2.4G/5G RF input/output port 1
46	GND	GND	Ground
47	GND	GND	Ground
48	NC	NC	Not Connected
49	NC	NC	Not Connected
50	NC	NC	Not Connected
51	NC	NC	Not Connected
52	GND	GND	Ground
53	GND	GND	Ground
54	WL_RF0	I/O	WIFI 2.4/5GHz RF input/output port 0
55	GND	GND	Ground
56	GND	GND	Ground
57	PMU_EN	I	Power Management Unit Enable
58	GND	GND	Ground
59	NC	NC	Not Connected
60	GND	GND	Ground
61	NC	NC	Not Connected
62	USB_DP	I/O	USB D+ Signal
63	USB_DN	I/O	USB D- Signal
64	NC	NC	Not Connected
65	NC	NC	Not Connected
66	VDD_3V3	PI	3.3 V supply for Power
67	GND	GND	Ground
68	WL_EN	I	WLAN enable signal. Active high is low in reset.
69	BT_EN	I	Bluetooth enable signal. Active high is low in reset.
70	GND	GND	Ground
71	VDDIO	PI	1.8 V supply
72	BT_UART_RTS	I/O	UART request-to-send. Active- low request-to-send signal for the HCI UART interface
73	BT_UART_CTS	I/O	UART clear-to-send Active-low request-to-send signal for the HCI UART interface.
74	BT_UART_TXD	O	UART serial output. Serial data output for the HCI UART interface.

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75	BT_UART_RXD	I	UART serial input. Serial data input for the HCI UART interface.
76	NC	NC	Not Connected
77	VDDIO	PI	1.8 V supply
78	GND	GND	Ground
79	NC	NC	Not Connected
80	GND	GND	Ground
81	GND	GND	Ground
82	GND	GND	Ground
83	VDDIO	PI	1.8 V supply
84	GND	GND	Ground
85	NC	NC	Not Connected
86	NC	NC	Not Connected
87	GND	GND	Ground
88	GND	GND	Ground
89	NC	NC	Not Connected
90	GND	GND	Ground
91	GND	GND	Ground
92	GND	GND	Ground
93	GND	GND	Ground
94	GND	GND	Ground
95	GND	GND	Ground
96	GND	GND	Ground
97	GND	GND	Ground
98	GND	GND	Ground
99	GND	GND	Ground
100	GND	GND	Ground
101	VDD_3V3	PI	3.3 V supply for Power
102	VDD_3V3	PI	3.3 V supply for Power
103	GND	GND	Ground
104	GND	GND	Ground
105	VDD_3V3	PI	3.3 V supply for Power
106	VDD_3V3	PI	3.3 V supply for Power
107	GND	GND	Ground
108	GND	GND	Ground
109	GND	GND	Ground
110	GND	GND	Ground
111	GND	GND	Ground
112	GND	GND	Ground

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3.3 Physical Dimension

3.3.1 Module dimension

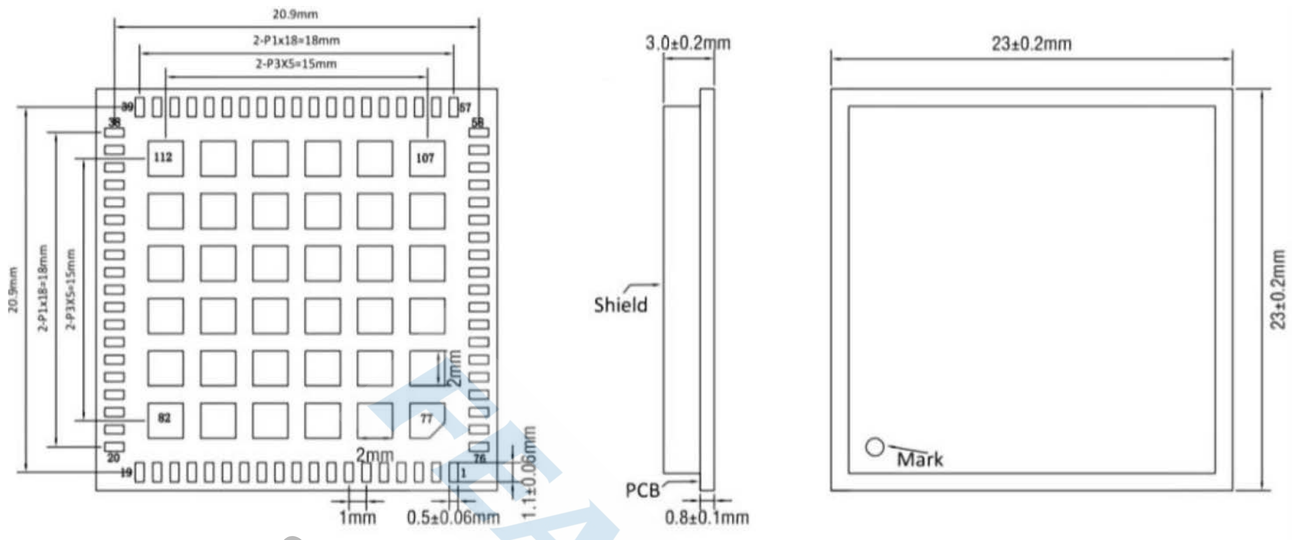

Figure 3-3-1: Module dimension

3.3.2 Recommended Module Mounting Pattern

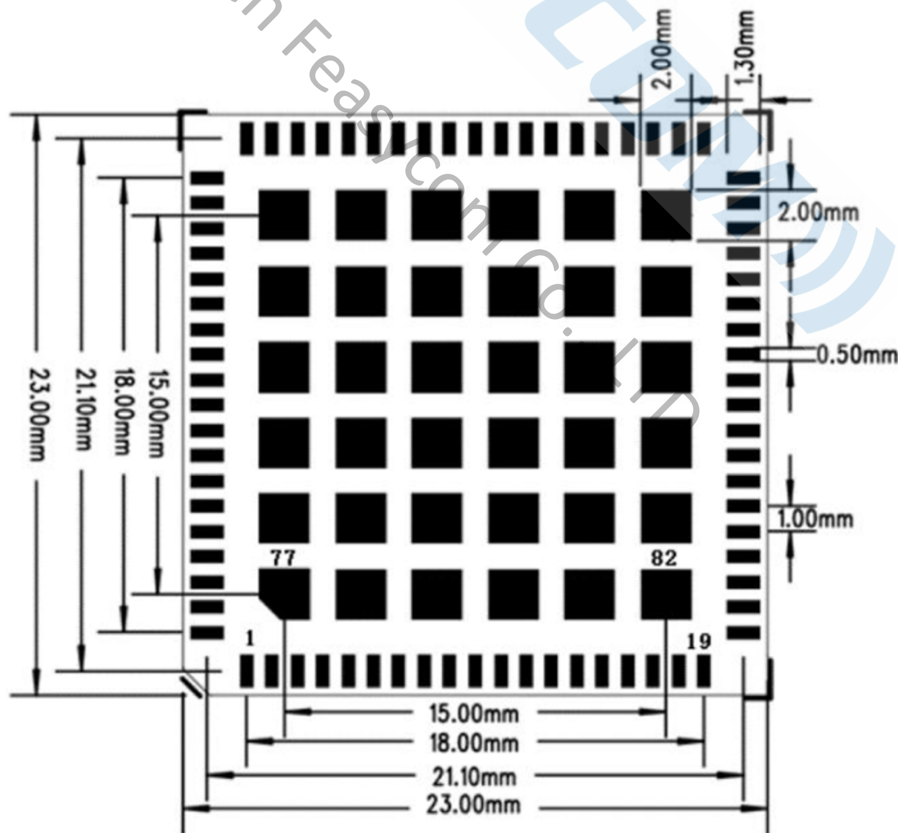

Figure 3-3-2: Recommended Module Mounting Pattern

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4 ELECTRICAL CHARACTERISTICS

4.1 Absolute maximum ratings

Table 4-1： Absolute maximum ratings

Parameter	Min	Type	Max	Unit
VDD_3V3(Buck Power Supply)	-0.3	3.3	3.63	V
VDDIO(DC supply voltage for digital I/O)	-0.3	1.8	1.98	V
Operating temperature range	-40		+85	℃
Storage temperature range	-40		+85	℃
ESD Stress Voltage To be updated after the completion of QUAL (Human Body Model)	-2000		+2000	V

4.2 General Requirements and Operation

Table 4-2： General Requirements and Operation

Parameter	Symbol	Min	Type	Max	Unit
VDD_3V3	VDD_3V3	2.97	3.3	3.63	V
VDDIO	VDDIO	1.71	1.8	1.89	V
VDD_3V3	Imax		3		A
VDDIO	Imax		500		mA

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5 Module RF Performances

5.1 WLAN Performances

5.1.1 WLAN 2.4GHz Receiver Characteristics

Table 5-1-1： WLAN 2.4GHz Receiver Characteristics

Parameter	Condition	Std	Unit
Test frequency		2412,2437,2462	MHz
Sensitivity 11b At < 8% PER limit; 11a/g/n OFDM At < 10% PER limit	1Mbps DSSS	<-92	dBm
	11Mbps CCK	<-84	dBm
	6Mbps OFDM	<-89	dBm
	54Mbps OFDM	<-71	dBm
	MCS0 20MHz	<-88	dBm
	MCS7 20MHz	<-69	dBm
	MCS0 40MHz	<-85	dBm
	MCS7 40MHz	<-65	dBm
11ax OFDMA At < 10% PER limit	MCS0 20MHz	<-88	dBm
	MCS11 20MHz	<-58	dBm
	MCS0 40MHz	<-85	dBm

		MCS11 40MHz	<-55	dBm

5.1.2 WLAN 2.4GHz Transmitter Power

Table 5-1-2: WLAN 2.4GHz Transmitter Power

Parameter		Condition	Std	Unit
Output Power		Test frequency	2412,2437,2462	MHz
	11B	1Mbps DSSS	16～20	dBm
		11Mbps CCK	16～20	dBm
	11G	6Mbps OFDM	12～18	dBm
		54Mbps OFDM	12～16	dBm
	11N	HT20 MCS0	10～16	dBm
		HT20 MCS7	10～16	dBm
		HT40 MCS0	12～18	dBm
		HT40 MCS7	10～16	dBm
	11AX	HE20 MCS0	12～18	dBm
		HE20 MCS11	10～16	dBm
		HE40 MCS0	12～18	dBm
		HE40 MCS11	10～16	dBm

5.1.3 WLAN 2.4GHz Transmitter EVM

Table 5-1-3: WLAN 2.4GHz Transmitter EVM

Parameter		Condition	Std	Unit
EVM(Measured by RMS)		Test frequency	2412,2437,2462	MHz
	11B	1Mbps DSSS	<-10	dB
		11Mbps CCK	<-10	dB
	11G	6Mbps OFDM	<-5	dB
		54Mbps OFDM	<-25	dB
	11N	HT20 MCS0	<-5	dB
		HT20 MCS7	<-27	dB
		HT40 MCS0	<-5	dB
		HT40 MCS7	<-29	dB
	11AX	HE20 MCS0	<-5	dB
		HE20 MCS11	<-35	dB
		HE40 MCS0	<-5	dB
		HE40 MCS11	<-35	dB

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5.2 WLAN 5G Radio Characteristics

5.2.1 WLAN 5G Rx RF Characteristics

Table 5-2-1： WLAN 11a-5G Rx RF Characteristics

Parameter	Condition	Std	Unit
Sensitivity (11a/n/ac PER limit < 10%)	Test frequency	5180,5500,5805	MHz
	6Mbps OFDM 1K	<-88	dBm
	54Mbps OFDM 1K	<-70	dBm
	HT20 MCS0	<-87	dBm
	HT20 MCS7	<-68	dBm
	VHT20 MCS8	<-64	dBm
	Test frequency	5190,5510,5795	MHz
	HT40 MCS0	<-84	dBm
	HT40 MCS7	<-65	dBm
	VHT40 MCS9	<-59	dBm
	Test frequency	5210,5530,5745	MHz
	HT80 MCS0	<-81	dBm
	HT80 MCS7	<-62	dBm
	VHT80 MCS9	<-56	dBm
Sensitivity (11ax PER limit < 10%)	Test frequency	5180,5500,5805	MHz
	HE20 MCS0	<-88	dBm
	HE20 MCS11	<-57	dBm
	Test frequency	5190,5510,5795	MHz
	HE40 MCS0	<-84	dBm
	HE40 MCS11	<-54	dBm
	Test frequency	5210,5530,5745	MHz
	HE80 MCS0	<-81	dBm
	HE80 MCS11	<-50	dBm

5.2.2 WLAN 5GHz Transmitter Power

Table 5-2-2： WLAN 5GHz Transmitter Power

Parameter	Condition	Std	Unit
Output Power	Test frequency	5180,5500,5805	MHz
	6Mbps	14～20	dB
	54Mbps	12～18	dB
	MCS0 20MHz	14～20	dB
	MCS7 20MHz	12～18	dB
	Test frequency	5190,5510,5795	MHz
	MCS0 40MHz	14～20	dB

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	MCS7 40MHz	12～18	dB
	Test frequency	5210,5530,5745	MHz
	MSC0 80MHz	14～20	dB
	MCS9 80MHz	10～18	dB

5.2.3 WLAN 5GHz Transmitter EVM

Table 5-2-3：WLAN 5GHz Transmitter EVM

Parameter	Condition	Std	Unit
EVM(Measured by RMS)	Test frequency	5180,5500,5805	MHz
	6Mbps	<-5	dB
	54Mbps	<-25	dB
	MCS0	<-5	dB
	MCS7	<-27	dB
	Test frequency	5190,5510,5795	MHz
	MCS0 40MHz	<-5	dB
	MCS7 40MHz	<-27	dB
	Test frequency	5210,5530,5745	MHz
	AX MCS11 80MHz	<-35	dB

5.3 WLAN 6G Radio Characteristics

5.3.1 WLAN 6GHz Rx RF Characteristics

Table 5-3-1：WLAN 6GHz Rx RF Characteristics

Parameter	Condition	Std	Unit
Sensitivity (11a/n/ac PER limit < 10%)	Test frequency	5955,6435,6995	MHz
	6Mbps OFDM	<-86	dBm
	54Mbps OFDM	<-68	dBm
	HT20 MCS0	<-85	dBm
	HT20 MCS7	<-68	dBm
	VHT20 MCS8	<-62	dBm
	Test frequency	5965,6445,7005	MHz
	HT40 MCS0	<-82	dBm
	HT40 MCS7	<-63	dBm
	VHT40 MCS9	<-57	dBm
	Test frequency	5985,6465,7025	MHz
	HT80 MCS0	<-79	dBm
	HT80 MCS7	<-60	dBm
	VHT80 MCS9	<-54	dBm
Sensitivity	Test frequency	5955,6435,6995	MHz

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(11ax PER limit < 10%)	HE20 MCS0	<-86	dBm
	HE20 MCS11	<-55	dBm
	Test frequency	5965,6445,7005	MHz
	HE40 MCS0	<-82	dBm
	HE40 MCS11	<-52	dBm
	Test frequency	5985,6465,7025	MHz
	HE80 MCS0	<-78	dBm
	HE80 MCS11	<-48	dBm

5.3.2 WLAN 6GHz Transmitter Power

Table 5-3-2： WLAN 6GHz Transmitter Power

Parameter	Condition	Std	Unit
Output Power	Test frequency	5955,6435,6995	MHz
	6Mbps	14～20	dB
	54Mbps	10～18	dB
	MCS0 20MHz	12～18	dB
	MCS11 20MHz	7～12	dB
	Test frequency	5965,6445,7005	MHz
	MCS0 40MHz	12～18	dB
	MCS11 40MHz	7～12	dB
	Test frequency	5985,6465,7025	MHz
	MSC0 80MHz	12～18	dB
	MCS11 80MHz	7～12	dB

5.3.3 WLAN 6GHz Transmitter EVM

Table 5-3-3： WLAN 5GHz Transmitter EVM

Parameter	Condition	Std	Unit
EVM(Measured by RMS)	Test frequency	5955,6435,6995	MHz
	6Mbps	<-5	dB
	54Mbps	<-25	dB
	MCS0	<-5	dB
	MCS7	<-27	dB
	Test frequency	5965,6445,7005	MHz
	MCS0 40MHz	<-5	dB
	MCS11 40MHz	<-27	dB
	Test frequency	5985,6465,7025	MHz
	AX MCS11 80MHz	<-35	dB

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5.4 BT Performance

5.4.1 BT Performance

Table 5-4-1: BT Performance

Parameter	Description	Min	Typ	Max	Unit
RF output power	At maximum power output level	-	-	11.5	dBm
Gain step		2	5	8	dB
Modulation characteristics	Δf1avg	140	157	175	KHz
	Δf2max(least 99.9% of all Δf2max)	115	145	-	KHz
	Δf1avg/Δf2avg	0.8	0.98	-	KHz
ICFT	Initial carrier frequency tolerance	-75	±18	+75	KHz
Carrier frequency drift	One slot packet (DH1)	-25	±10	-25	KHz
	Two slot packet (DH3)	-40	±10	-40	KHz
	Five slot packet (DH5)	-40	±10	-40	KHz
	Max drift rate		10	20	KHz/50us
TX output spectrum	20dB bandwidth		922	1000	KHz
In-Band spurious emission	±2MHz offset		-38	-20	dBm
	±3MHz offset		-43	-40	dBm
	>±3MHz offset		-45	-40	dBm

5.4.2 BT EDR Performance

Table 5-4-2: BT EDR Performance

Parameter	Description		Min	Typ	Max	Unit
Maximum transmit power	π/4 DQPSK		-	8.5	-	dBm
	8PSK		-	8.5	-	dBm
Relative transmit power	π/4 DQPSK		-	-3	-	dB
	8PSK		-	-3	-	dB
Frequency stability	Maximum carrier frequency stability, ω0	π/4 DQPSK	-10	±4	10	KHz
		8PSK	-10	±4	10	KHz
	Maximum carrier frequency stability, ω1	π/4 DQPSK	-75	±18	75	KHz
		8PSK	-75	±18	75	KHz
	Maximum carrier frequency stability,| ω0+ω1|	π/4 DQPSK	-75	±20	75	KHz
		8PSK	-75	±20	75	KHz
Modulation accuracy	RMS DEVM	π/4 DQPSK	-	8	20	%
		8PSK	-	8	12	%
	99% DEVM	π/4 DQPSK	-	11	-	%
		8PSK	-	11	-	%
	Max drift rate	π/4 DQPSK	-	15	35	%

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		8PSK	-	15	25	%
In-Band spurious emission	±1MHz offset	π/4 DQPSK	-	-29	-26	dB
		8PSK	-	-29	-26	dB
	±2MHz offset	π/4 DQPSK	-	-23	-20	dB
		8PSK	-	-23	-20	dB
	>±3MHz offset	π/4 DQPSK	-	-40	-40	dB
		8PSK	-	-40	-40	dB

5.4.3 BT BLE Performance

Table 5-4-3: BT BLE Performance

Parameter	Description		Min	Typ	Max	Unit
output power	BLE 1Mbps		-	11	-	dBm
	BLE 2Mbps		-	11	-	
Carrier Frequency Offset and Dirft	Frequency offset	BLE 1Mbps	-150	±10	150	KHz
		BLE 2Mbps	-150	±10	150	KHz
	Frequency drift	BLE 1Mbps	-50	±10	50	KHz
		BLE 2Mbps	-50	±10	50	KHz
	Max. drift rate	BLE 1Mbps	-20	±10	20	KHz
		BLE 2Mbps	-20	±10	275	KHz
Modulation characteristics	Δf1avg	BLE 1Mbps	225	250	-	%
		BLE 2Mbps	450	500	-	%
	Δf2max(least 99.9% of all Δf2max)	BLE 1Mbps	185	225	-	%
		BLE 2Mbps	370	450	-	%
	Δf1avg/Δf2avg	BLE 1Mbps	0.8	0.9	-	%
		BLE 2Mbps	0.8	0.9	-	%
In-Band spurious emission	±2MHz offset, ±4MHz, ±5MHz offset	BLE 1Mbps	-	-35	-20	dB
		BLE 2Mbps	-	-35	-20	dB
	>±3MHz offset, >±6MHz offset	BLE 1Mbps	-	-40	-30	dB
		BLE 2Mbps	-	-40	-30	dB

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6 Wi-Fi subsystem

6.1 Wi-Fi MAC

6.1.1 Features

Wi-Fi MAC supports the following features:

- Support all date rates of 802.11a/g including 6, 9, 12,18, 24,36,48 and 54Mbps.
- Support short Gl and all data rates of 802.11n including MCS0 to MCS7.

- Support 802.11ac MCS0 to MCS9.
- Support 802.11ax MCS0 to MCS11.
- AMPDU/AMSDU RX (de-aggregation) and Tx (aggregation)support.
- TX beaformer and RX beamformer.
- TX rate adaptation.
- TX power control.
- Security
  - 64-bit WEP (WEP-40) and 128-bit WEP(WEP-104) encryption with hardware TKlP and CKlP processing.
  - AES-CCMP hardware processing.
  - GCMP hardware processing.
- Support 2x2 and two independent 1x1 operations.
- Low power beacon filtering.
- Management/control frame filtering.

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6.2 WLAN Baseband

6.2.1 Features

Wi-Fi baseband supports the following features:

- 20/40/80 MHz channels mode.
- Dual band dual concurrent(DBDC)
- Two Wi-Fi ports can work on two different bands (A-band and G-band) concurrently.
- Use WF0 for A-band, and WF1 for G-band for better performance.
- HE MCS0-11 BW20/40/80MHz with Nss=1~2.
- Short Guard Interval.
- Space-time block code (STBC).
- Low Density Parity check (LDPC).
- Support digital pre-distortion to enhance PA performance.
- Smoothing (channel estimation) extension to MIMO case.
- DFS radar detection.
- Beamformer (explicit/implicit).
  - Decoded BW20/40/80 up to 2x2 BF matrix apply.
- Beamformer.

- Decoded BW20/40/80 up to 4x2 Mu matrix feedback.
- DBDC up to 4x1 MU matrix feedback, A-band BW20/40/80, G-band Bw20/40.

- MU-MIMO RX (MU capable STA only, can't be AP for DL-MU-MIMO).
- Support 2x2 and two independent 1x1 operations.
- 802.11v location.
- Support up to 1024QAM.

6.3 WLAN RF

6.3.1 Features

RF supports the following features:

- Integrated 2.4GHz/5GHz/6GHz PA and LNA, and T/R switch.
- Integrated 2.4GHz/5GHz/6GHz Balun.
- Support2,4GHz/5GHz/6GHz external PA and LNA.
- Support frequency band
  - 2.4GHz: 2412-2484MHz
  - 5GHz:4905-5915MHz
  - 6GHz:5930-7110MHz
- Configurable PA that provides different PA modes at different power levels for power consumption Optimization.

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7 Bluetooth subsystem

7.1 Feature set

Bluetooth supports the following features:

- Bluetooth 5.4
  - LE 2M PHY and LE Coded PHY.
  - LE Extended Advertising and Periodic Advertising.
  - LE high duty cycle non-connectable ADV.
  - Channel Selection Algorithm #2.
  - Angle of Arrival (AoA) and Angle of Departure (AoD).

- Connected Isochronous Stream master and slave.
- Isochronous Broadcaster and Synchronized Receiver.

- Compatible Bluetooth 4.2
  - LE privacy 1.2.
  - LE Data Packet Length Extension.
  - LE security connection.
- Single-ended, RF port with integrated Balan and T/R switch.
- Integrated high efficiency PA and TSSI.
- Baseband and radio BDR and EDR packet types: 1Mbps (GFSK), 2Mbps (π /4-DQPSK), and 3Mbps (8PSK).
- Fully functional Bluetooth baseband: AFH, forward error correction, header error control, access code correlation, CRC, whitening.
- Standard pairing, authentication, link key, and encryption operation.
- Standard power saving mechanisms: sniff mode and sniff-subrating.
- Interlaced scan for faster connection setup.
- Up to 7 simultaneous active ACL connections with background inquiry and page scan.
- Up to 16 BLE links.
- Scatternet support.
- Channel quality driven data rate control.
- WB RSSI support. Monitor environment air condition to select good channel for AFH.

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8 Reliability Test

8.1 Item of Reliability Test

Table 8-1-1: Item of Reliability Test

Test Item	Specification
High Temperature (Storage)	Place 96 hours at 90˚C environment, and 2 hours at normal temperature and humidity then test, module should meet the standard of chapter 6.2.
Low Temperature (Storage)	Place 96 hours at 90˚C environment, and 2 hours at normal temperature and humidity then test, module should meet the standard of chapter 6.2.
High Humidity (Storage)	At the temperature of +60˚C, 90%RH environment for 96 hours, and 2 hours at normal temperature and humidity, then test, module should meet the standard of chapter 6.2.
High Temperature (Operating)	At the temperature of +60˚C, 90%RH environment for 96 hours, and 2 hours at normal temperature and humidity, then test, module should meet the standard of chapter 6.2.

Low Temperature (Operating)	Module must be able to work continuously for 96 hours at t the environment of -40°C , The module should work normal within the time or module should meet the standard of chapter 6.2 .
High and low temperature cycling test	Tstg Max 85°C 30 min s, Temperature shift time: within 2hrs. Tstg Min -40°C 30 min, Repeat 10 cycles. The module should be cold to normal temperature for two hours, module should meet the standard of chapter 6.2.
Vibration Resistance	Freq: 10~200Hz, 0.1 oct/min, max acceleration: 2.5Grms-Test time: X, Y, Z axis for 6 hours. After 1 hour vibration test, do the test in each direction. In normal temperature condition, take measurements within 3 hours. Module should meet the standard of chapter 6.2.
Shock Test	Shock Test: Impact acceleration: 70G(m/sec2), impact time: 11 mS, impact frequency and direction: 10 times each in 6 directions. In normal temperature condition, take measurements within 3hr， Module should meet the standard of chapter 6.2.
Electrostatic Resistance	Human body model, C=100pF, R=1.5kΩ, ±2kV, INT=0.5S/3times, Take measurements after 2hours in normal condition (Only for shield case and GND).

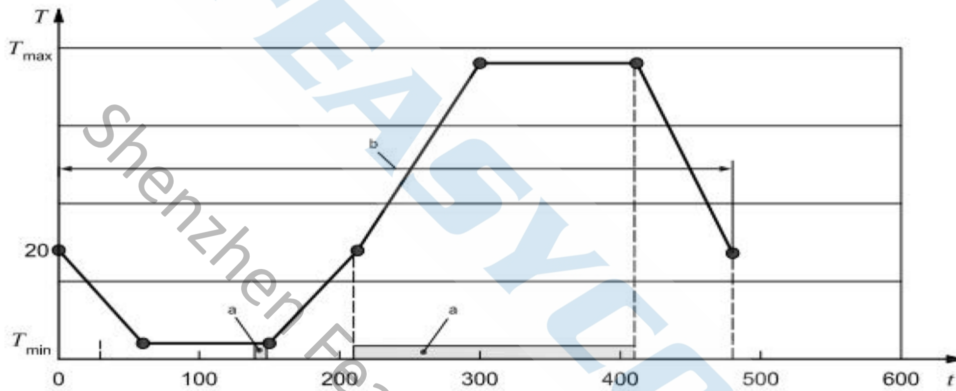

Figure 8-1-1: Temperature cycles with specified change rate

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Table 8-1-2：Temperature cycles with specified change rate

Key	
T	temperature, in *C
t	time, in min
T_{min}	minimum operating temperature, in ° C (see Table 1)
T_{max}	maximum operating temperature, in ° C (see Table 1)
a	Operating mode 3.2 in accordance with ISO 16750-1.
b	One cycle

Table 8-1-3：Temperatures and time duration for temperature cycling (see Figure 6-1-1)

Time(min)	**Temperature°C**
0	20
60	T_{min}
150	T_{min}
2110	20
300	T_{max}

410	T_{max}
480	20
NOTE Codes are in accordance with Table 1 (codes A to T). in the vehicle environment, some equipment might experience different conditions regarding temperatures, temperature gradients and duration: in all these cases, code Z is used。	

8.2 Reliability Test Standard

Table 8-2-1：WLAN 2.4G Performance

Item	Condition	mode	rate	Unit	Std
Transmitter Power	@2412/2437/2462MHz	DSSS CCK	11Mbps 54Mbps	dBm dBm	13~20 12~16
EVM	@2412/2437/2462MHz	DSSS	1Mbps 54Mbps	dB dB	≦-10 ≦-25
Receiver sensitivity	At < 10% PER limit @2412/2437/2462MHz	11b mode： DSSS （PER<8%） 11g mode： OFDM （PER<10%）	11Mbps 54Mbps	dBm dBm	≦-84 ≦-71

Table 8-2-2：WLAN 5G Performance

Item	Condition	mode	rate	Unit	Std
Transmitter Power	@5210/5530/5745MHz	11ac OFDM	MCS9	dBm	10~15
EVM	@5210/5530/5745MHz	11ac OFDM	MCS9	dB	≦-32
Receiver sensitivity	@5210/5530/5745MHz	11ac OFDM	MCS9	dBm	≦-56

Table 8-2-3：WLAN 6G Performance

Item	Condition	mode	rate	Unit	Std
Transmitter Power	@5985/6465/7025MHz	11ax OFDM	MCS11	dBm	7~12
EVM	@5985/6465/7025MHz	11ax OFDM	MCS11	dB	≦-35
Receiver sensitivity	@5985/6465/7025MHz	11ax OFDM	MCS11	dBm	≦-48

Table 8-2-4：BT Performance

Parameter	Condition	Std	Unit
Test frequency	2402(Channel0) 2441(Channel39) 2480(Channel78)		MHz
BR Output Power		-6～20	dBm
single/ multi slot packets Sensitivity (Power=-70dBm)	Power-70dBm	BER⩽ 0.1%	

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9 PHYSICAL INTERFACE

9.1 Power on and Power off Sequence

The figure below shows the chip power-on sequence.

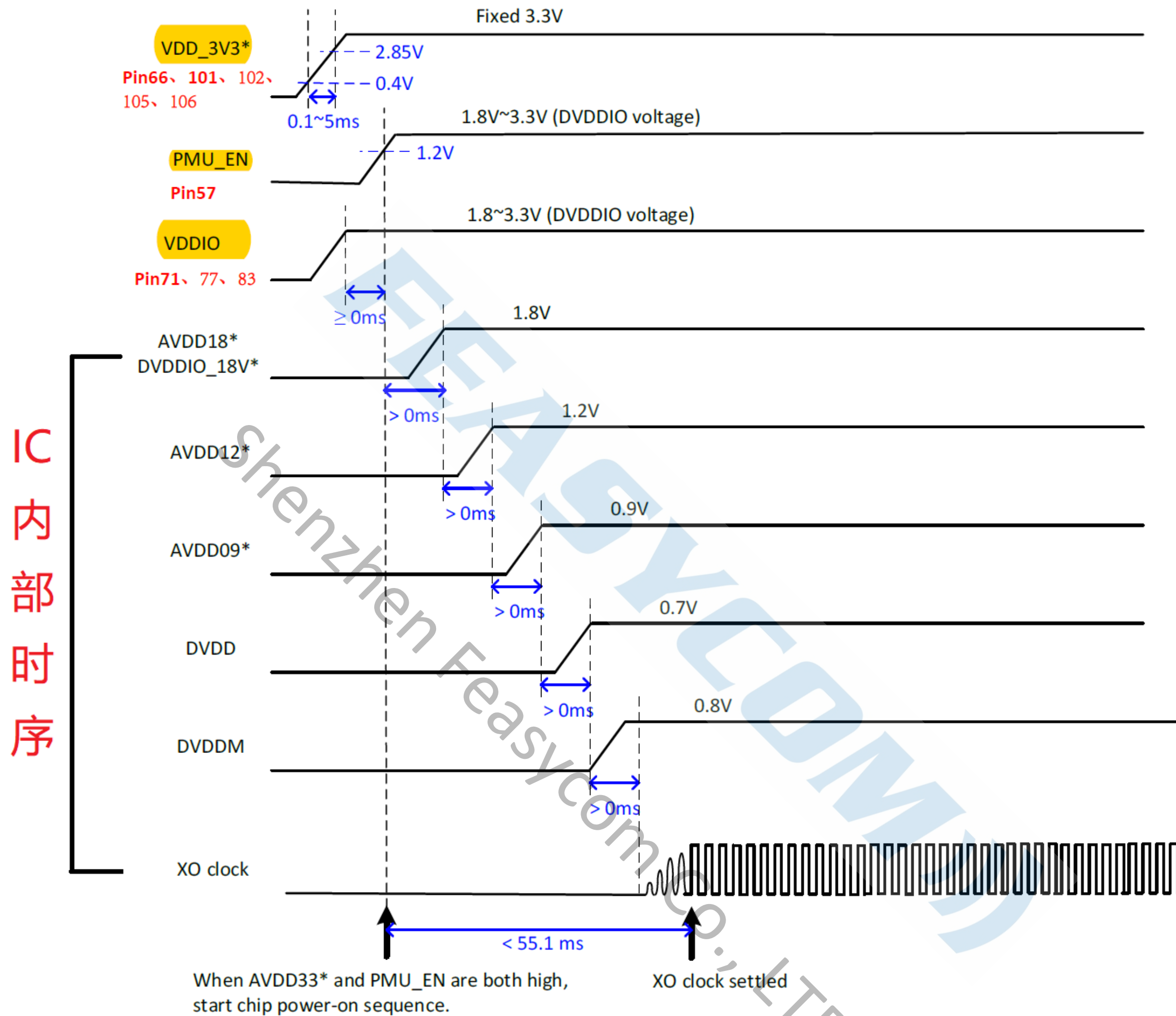

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Figure 9-1-1: Power on and Power off Sequence

Table 9-1-1： Power-on timing parameters

Symbol	Description	Min	Max	Units
t1	PIN66、101、102、105、106 3.3V Start ramping-up	0		us
t2	PIN71、88 and PIN83 1.8V start ramping-up	10		us
t3	PIN57　PMU_EN（Is pulled up by 3V3 inside the module）	10		us

9.2 PCIE Express Interface

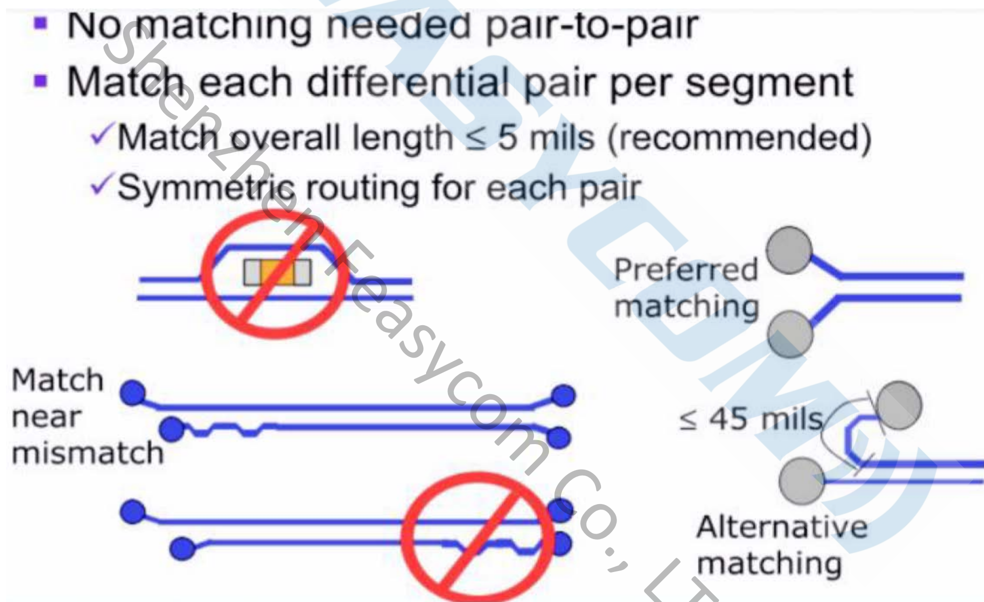
The PCI Express (PCIE) core on the IC is a high-performance serial I/O interconnect that is protocol compliant and electrically compatible with the PCI Express Base Specification v3.0 running at Gen2 speeds. This core contains all the necessary blocks, including logical and electrical functional subblocks to perform PCIE functionality and maintain high-speed links, using existing PCI system configuration software implementations without modification.

9.3 PCB Layout Recommendation

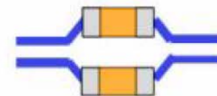
1.PCIE layout guide

The following PCIE routes must comply with the following rules to prevent overshoot/undershoot, because these routes drive 8mA PCIE_CLK_P & PCIE_CLK_N, PCIE_TX_P & PCIE_TX_N, PCIE_RX_P & PCIE_RX_N.

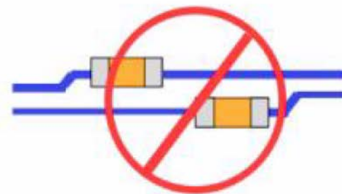
These pins are differential signals. The path length of these signals is less than 15 CM and the line impedance is less than 100Ω.



- Size: 0402 best, 0603 ok
- No 0805 size or C-packs
- Symmetric placement best



- Cap size: 0.1uF best
- Same sizes for both D+/D-
- Cap location:
  - ✓Along Tx pairs on system board
  - ✓Along Tx pairs on add-in card



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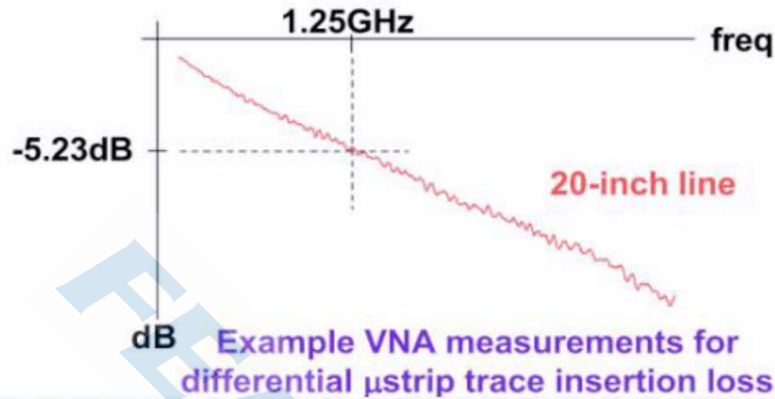

2.HCI Lines Layout Guide

The following HCI line routing must comply with the following rules to prevent overshoot or undershoot, because these routes drive 4 to 8 mA.

BT_UART_RTS

BT_UART_CTS

BT_UART_TXD

BT_UART_RXD

The route length of these signals is less than 15 cm. Line impedance less than 50Ω.

3.PCM Lines Layout Guide

The process routing of the following PCM lines must comply with the following rules to prevent overshoot/undershoot as these lines drive 4 mA.

PCM_IN

PCM_OUT

PCM_CLK

PCM_SYNC

The route length of these signals is less than 15 cm. Line impedance less than 50Ω.

9.4 UART Parameters

Table 9-4-1： UART Parameters

Parameter	Value
Number of data bits	Eight
Parity bit	No parity

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Stop bit	One stop bit
Flow control	RTS/CTS (hardware)
Flow off response	Two bytes maximum
Supported transport bit rates (bps) [a]	9.6 K, 19.2 K, 38.4 K, 57.6 K, 115.2 K, 125 K, 230.4 K, 250 K, 460.8 K, 500 K, 720 K, 921.6 K, 1 M, 1.6 M, 2 M, 3 M, 3.2 M, with an accuracy of +1.5/-2.5%

[a] UART maximum baud rate is 3.2 Mbps.

- The recommended normal working range of Bluetooth UART Baud rate 115.2～3000 Kbps
- The UART baud rate associated with the use of the system platform, According to the system platform adjust Baud rate.

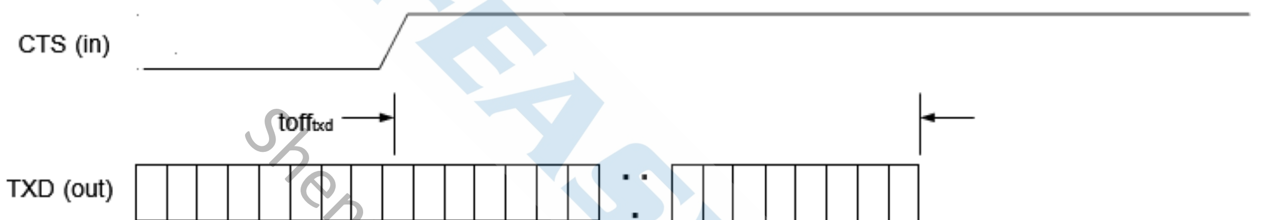

Figure 9-4-1: HCI UART transmit flow control timing

Table 9-4-2: HCI UART transmit flow control timing

Parameter	Description	Min.	Typ.	Max.	Unit
$toff_{txd}$	Delay from CTS to TXD stop			8	byte

The following figure and table show the HCI UART receive timing:

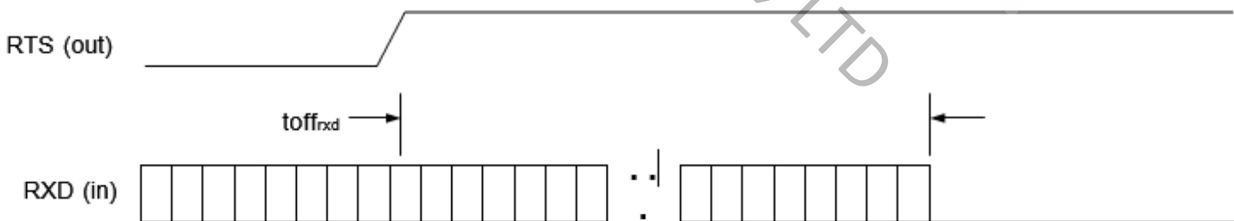

Figure 9-4-2: HCI UART receive flow control timing

Table 9-4-3: HCI UART receive flow control timing

Parameter	Description	Min.	Typ.	Max.	Unit
$toff_{txd}$	Delay from RTS to RXD stop			8	byte

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9.5 Bluetooth PCM interface

The pulse coded modulation (PCM) interface connects the MT7921AEN device to the phone's audio interface, or to peripheral devices, such as a codec. The PCM interface circuits use digital I/O pins that receive power from the VDDIO supply.

The MT7921AEN PCM interface has been designed to minimize audio latency. The following table lists the typical audio latencies for various packet types:

Table 9-5-1: Typical PCM interface audio latency

Packet type	Audio latency
HV3/EV3 T_{eSCO} = 6, W_{eSCO} = 0	4.4 ms
EV3 T_{eSCO} = 6, W_{eSCO} = 2	5.7 ms
EV3 T_{eSCO} = 6, W_{eSCO} = 4	6.9 ms

The PCM interface is configured to operate as master or slave. In each case, the PCM_IN pin is the data receive terminal (an input), and the PCM_OUT pin is the data transmit terminal (an output). The clock and sync pins function as inputs or outputs, depending on whether the MT7921AEN PCM interface is configured as a master or slave:

- When the MT7921AEN PCM interface is the master: PCM_CLK and PCM_SYNC are outputs from the MT7921AEN to the PCM bus slave(s).
- When the MT7921AEN PCM interface is the slave: PCM_CLK and PCM_SYNC are inputs to the MT7921AEN device from the PCM bus master.

The following table lists the PCM interface specifications:

Table 9-5-2: PCM interface specifications

Parameter	Description	Min.	Typ.	Max.	Unit
Clock rate (slave)	Determined by the master	64		2,048	kHz
Clock rate (master)	(32 MHz * N/4,000), in which N is an integer, 8 ≤ N ≤ 256	64		2,048	kHz
Frame size		1	8	256	Bits
Slot size		1	13	16	Bits
Slot number	Number of slots that can be configured per frame	1		32	Slots/frame

Example timing diagrams and specifications for slave and master configurations are described in the following figures and tables:

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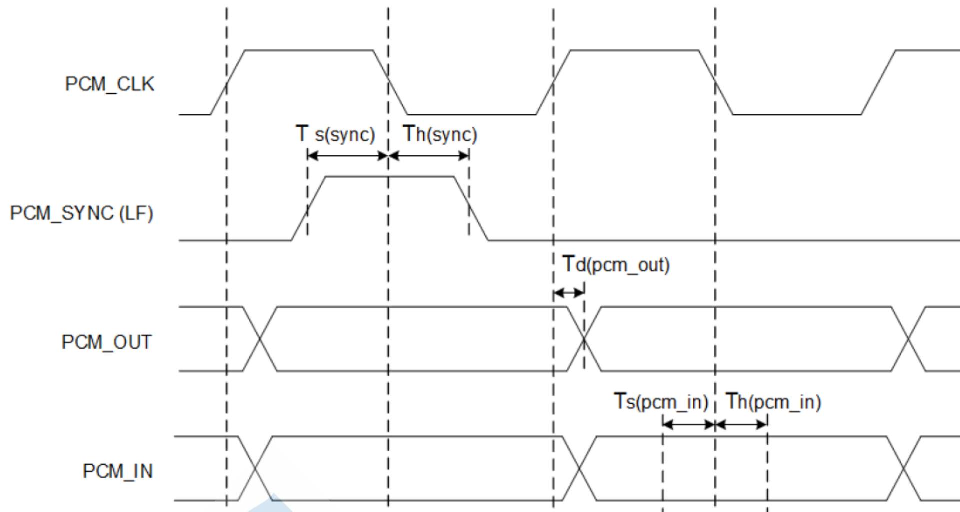

Figure 9-5-1: PCM interface timing diagram (slave)

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Table 9-5-3： PCM interface timing in slave mode

Symbol	Description	Min.	Typ.	Max.	Unit
F_{pcm_clk}	PCM_CLK frequency	64		2,048	kHz
Ts_{pcm_sync}	Setup time PCM_SYNC to PCM_CLK fall	0			ns
Th_{pcm_sync}	Hold time PCM_CLK fall to PCM_SYNC fall	150			ns
Td_{pcm_out}	Delay from PCM_CLK rise to PCM_OUT	0		150	ns
Ts_{pcm_in}	Setup time PCM_IN to PCM_CLK fall	0			ns
Th_{pcm_in}	Hold time PCM_IN after PCM_CLK fall	150			ns

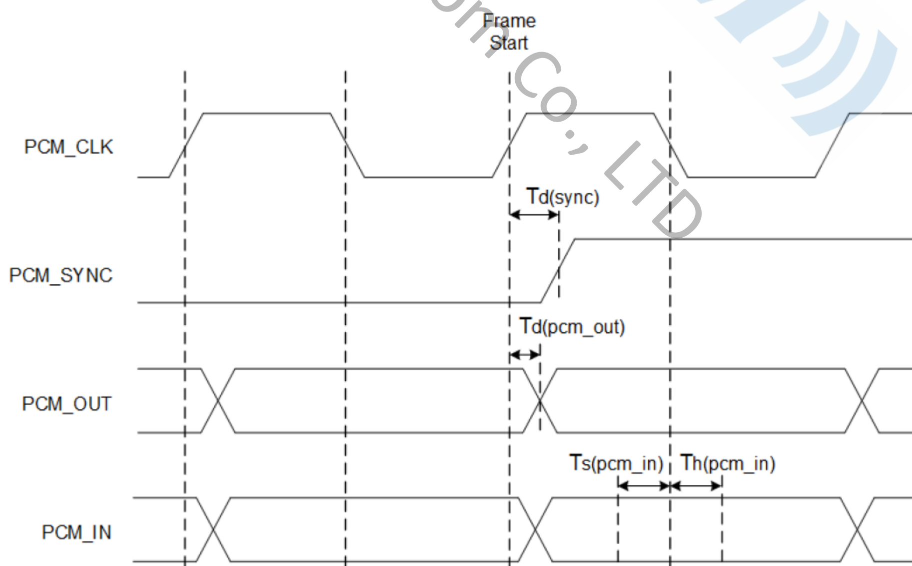

Figure 9-5-2: PCM interface timing diagram (master)

Table 9-5-4： PCM interface timing in slave mode

Symbol	Description	Min.	Typ.	Max.	Unit

F_{pcm_clk}	PCM_CLK frequency	64	2048	kHz
Ts_{pcm_sync}	Delay from PCM_CLK rise to long SYNC	-10	50	ns
Td_{pcm_out}	Delay from PCM_CLK rise to PCM_OUT	-10	50	ns
Ts_{pcm_in}	Setup time PCM_IN to PCM_CLK fall	50		ns
Th_{pcm_in}	Hold time PCM_IN after PCM_CLK fall	150		ns

9.6 I²S timing for slave

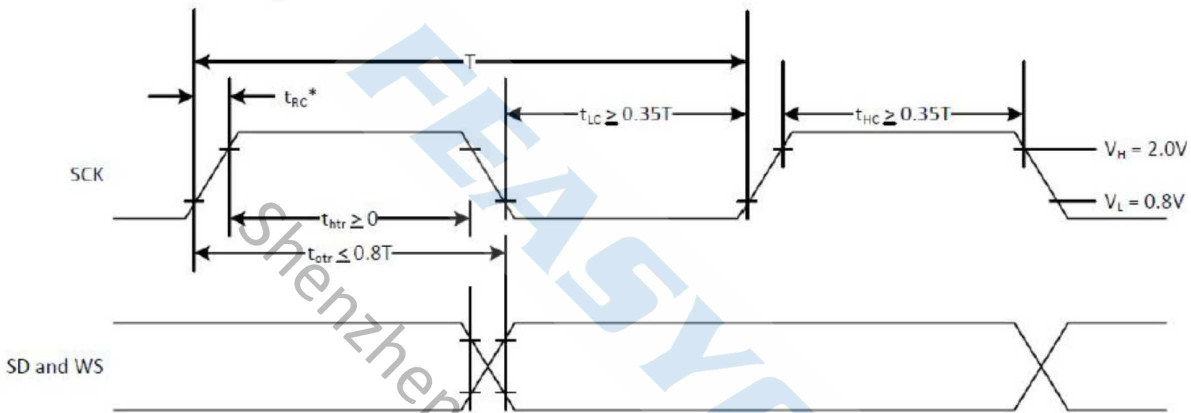

Figure 9-6-1: I²S Transmitters Timing

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T= Clock period

T_{tr}= Minimum allowed clock period for transmitter

$T=T_{tr}$

*t_{RC} is only relevant for transmitters in slave mode

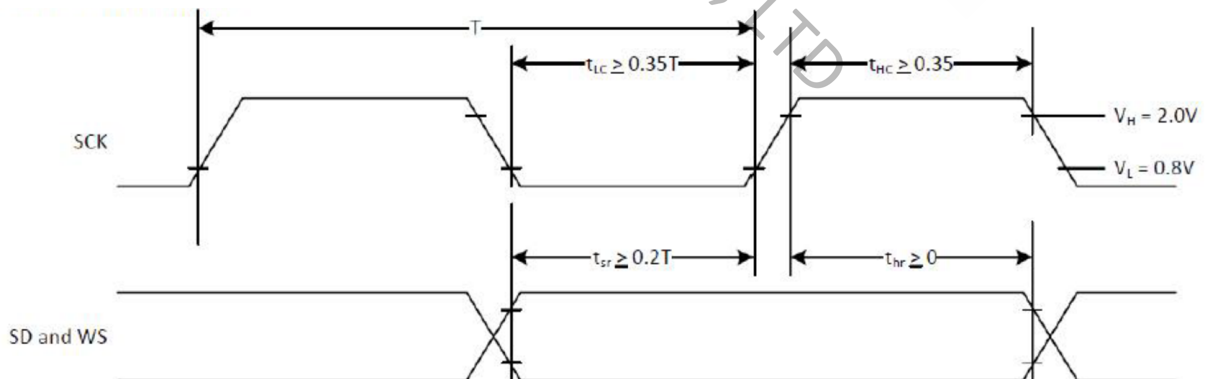

Figure 9-6-2: I²S Receiver Timing

T= Clock period

T_r= Minimum allowed clock period for transmitter

$T>T_r$

Table 9-6-1: Timing for I²S Transmitters and Receivers

	Transmitter				**Receiver**				
	Lower Limit		Upper Limit		Lower Limit		Upper Limit		
	Min	Max.	Min	Max.	Min	Max.	Min	Max.	Notes
Clock Period T	T_{tr}				T_r				a
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{Hc}	$0.35T_{tr}$				$0.35T_{tr}$				b
LOW_{Lc}	$0.35T_{tr}$				$0.35T_{tr}$				b
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{Hc}		$0.35T_{tr}$				$0.35T_{tr}$			c
LOW_{Lc}		$0.35T_{tr}$				$0.35T_{tr}$			c
Rise time t_{rc}			$0.15T_{tr}$						d
Transmitter									
Delay t_{dtr}				0.8T					e
Hold time t_{htr}		0							d
Receiver									
Setup time t_{sr}						$0.2T_r$			f
Hold time t_{hr}						0			f

10 MSL & ESD

Table 10-1: MSL and ESD

Parameter	**Value**
MSL grade:	MSL 3
ESD grade	Electrostatic discharge
ESD – Human Body Model (HBM) Rating JESD22-A114-B	Pass ±2000 V, All pins pass(exclude RF/HSS pin:1000V)
ESD – Charged Device Model (CDM) Rating JESD22-C101-D	Pass ±500 V, All pins pass(exclude RF/HSS pin:250V)

11 RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a

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new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Notice (注意) :

Feasycom module must use Step-Stencil, suggestion using the stencil thickness about 0.16-0.2mm, it could be modify with the product.

使用我司模块，须使用阶梯钢网，建议阶梯钢网厚度0.16-0.20mm，可根据自己产品适应性，进行相应调整.

Table 11-1: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

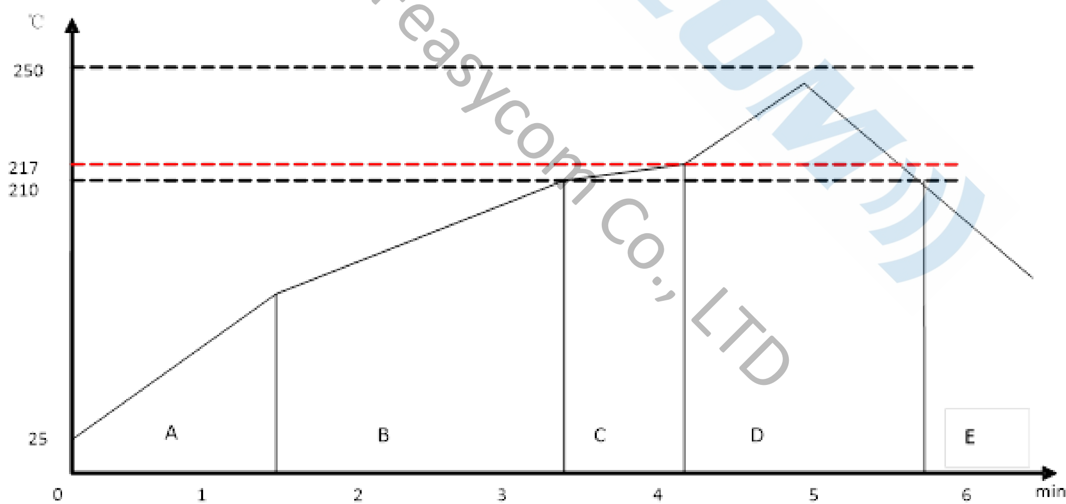

Figure 11-1：Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120**

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second for this zone.

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

12 MECHANICAL DETAILS

12.1 Mechanical Details

- Dimension: 23mm(W) x 23mm(L) x 3.0mm(H) Tolerance: ±0.2mm
- Module size: 23mm X 23mm Tolerance: ±0.2mm
- Pad size: 1.3mmX0.5mm Tolerance: ±0.1mm
- Pad pitch: 1.0mm Tolerance: ±0.1mm

(分板后边角残留板边误差：不大于 0.5mm) (Residual plate edge error: < 0.5mm)

TOP View

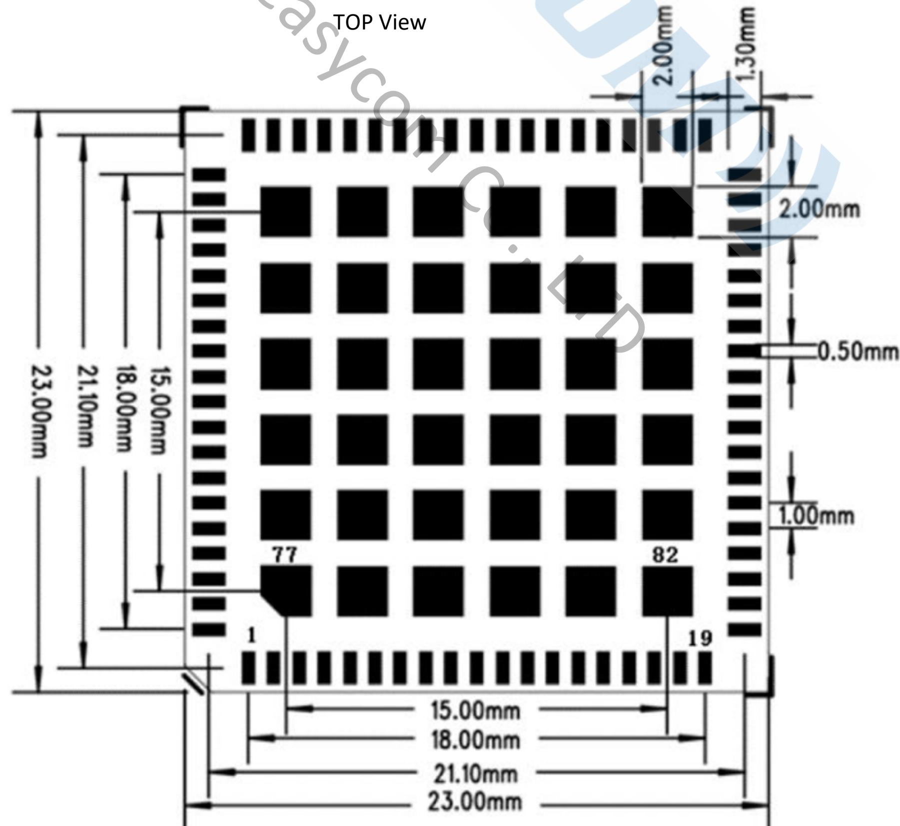

Figure 12-1：FSC-BW1501UV footprint Layout Guide (Top View)

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13 HARDWARE INTEGRATION SUGGESTIONS

13.1 Requirement for the 3.3V power supply

- To use a dedicated power supply circuit for Wi-Fi (and BT).
- <0.05% line regulation and <0.5%/A load regulation are required for ripple frequency below 100KHz.
- Transient-response: 1, The ripple raised from 100/800mA step-response test should be small than 200mVpp.

2, The ripple swing shall settle down within 1~2 cycles, 2 cycles for the worst case.

- Power supply spur: make sure the spurs from switching mode power supply or other noisy circuits are reasonably small. Once issue concerned with such a power supply spur, alternative power supply filtering might be needed.
- VDD_3V3: 3.0 to 3.6V (Peak Current 3A); VDDIO: 1.7 to 1.9V (Peak Current 500mA)

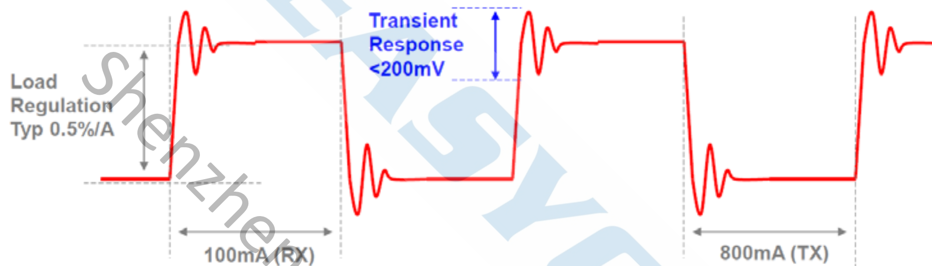

Figure 13-1: Requirement for the 3.3V power supply

13.2 Connections when BT's HCI is by UART

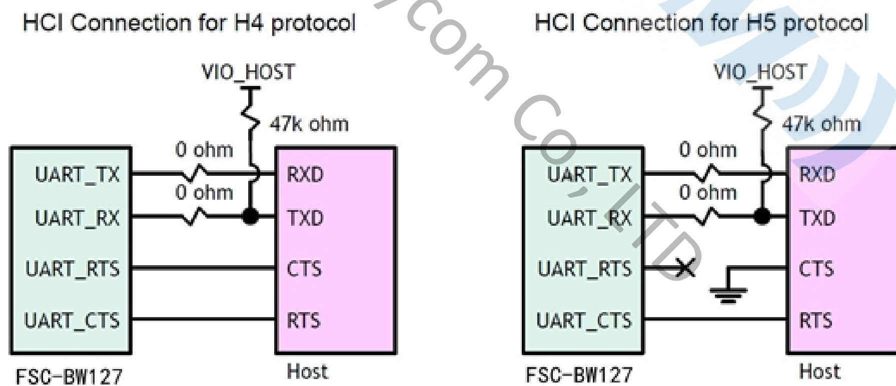

Figure 13-2: Connections when BT's HCI is by UART

Note:

1. Reserve a 47k pull-high resistor on host TXD when this port is not in output mode for default.

   (If not sure, reserve a 47k resistor is recommended for avoid TXD being floating)

2. There must be 0 ohm jumper-resistors on TX/RX paths, for BQB certification test.

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13.3 RF Circuit- RF pads

- Some RF components such as 0402-packaged RLC, connectors, or module pins are with large soldering pad, those pads have higher parasitic capacitance which can impact the characteristic impedance of RF traces.
- The GND under those pads shall be dug out, shown as below, for keeping good 50Ω matching.
- The dig-out layers and area should be calculated carefully, we recommend digging the area a little higher than the simulation results.

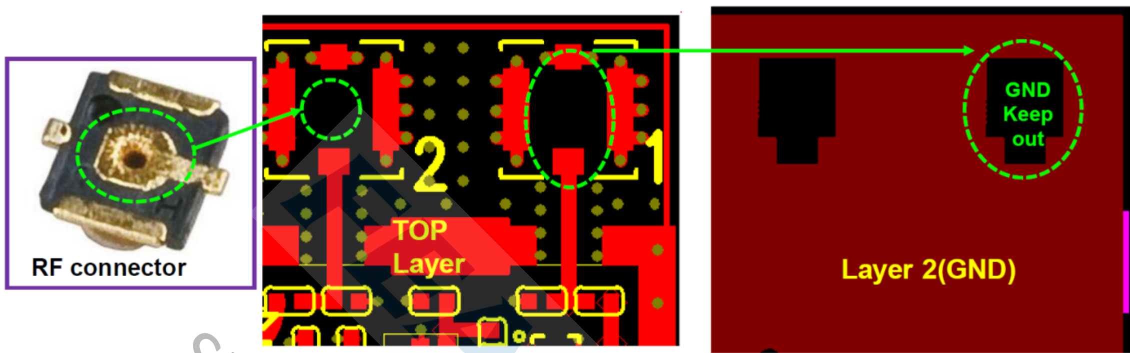

Figure 13-3: RF Circuit- RF pads

13.4 Recommendable antenna & IPEX by Feasycom

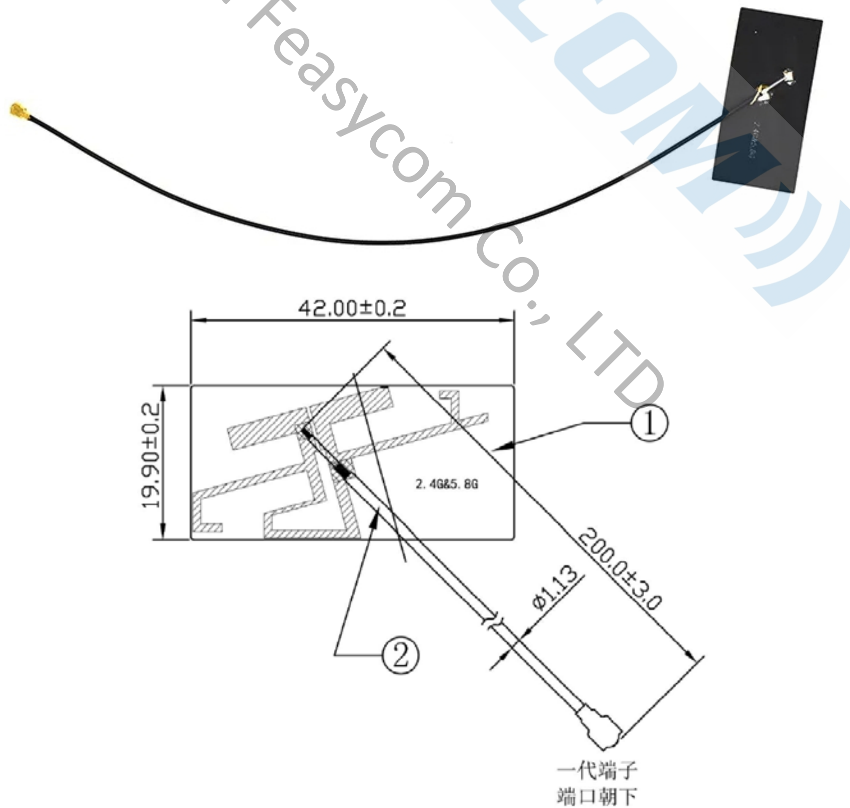

Figure 13-4-1: 2.4GHz & 5GHz Dual-band antenna, with IPEX first generation interface

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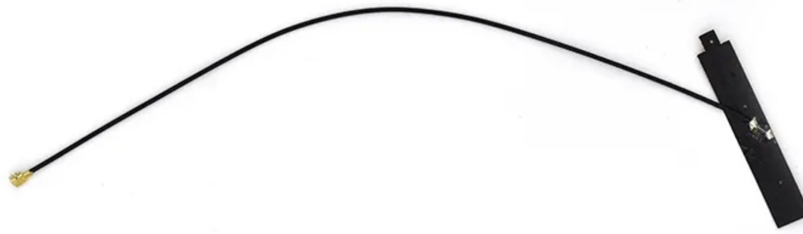

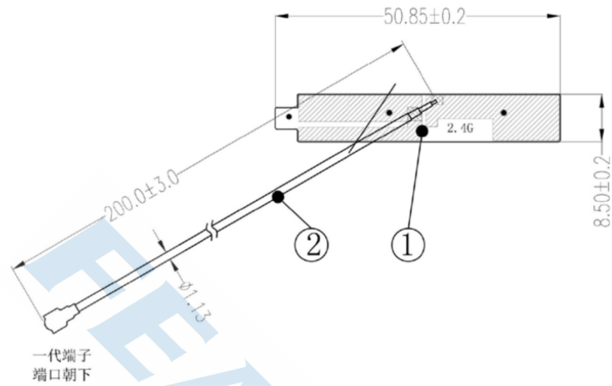

Figure 13-4-2: 2.4GHz antenna with IPEX first generation interface

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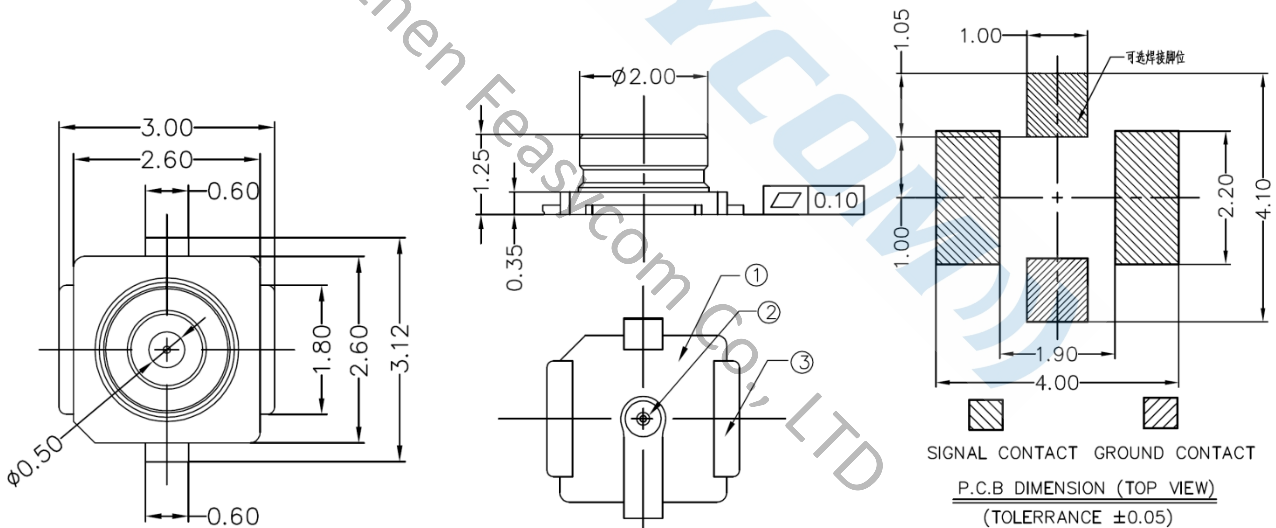

ITEM	NAME	Q'TY	MATERIAL ⚠1	FINISH ⚠2
3	GROUND CONTACT	1	JIS C5191-H	Au 1u" Min. over Ni 50~100u" Min.
2	CONTACT	1	JIS C2680-1/4H	Au 1u" Min. over Ni 50~100u" Min.
1	HOUSING	1	LCP E6808	UL94V-0,30% GF

NOTES:
1. FREQUENCY RANGE:
   DC TO 6GHZ (VSWR: 1.3MAX AT 0.1~3GHZ, 1.4MAX AT 3~6GHZ)
2. CHARACTERISTIC IMPEDANCE: 50 (NOMINAL);
3. TEMPERATURE: −40℃ TO +90℃;
4. RATED VOLTAGE : 60VAC;
5. CONTACT RESISTANCE :
   20m MAX.(SIGNAL CONTACT)
   20m MAX.(GROUND CONTACT)
6. WITHSTAND VOLTAGE : 200VAC FOR 1 MINUTE MIN;
7. INSULATION RESISTANCE : 500M MIN. AT 100VDC;
8. THIS COMPONENT IS HALOGEN FREE.

Figure 13-4-3: IPEX first generation interface

13.5 Soldering Recommendations

FSC-BW1501UV is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

13.6 Layout Guidelines (Internal Antenna)

Important Note: The antenna for FSC-BW1501UV is suggested to support both 2.4GHz and 5.8GHz dual frequency bands. We recommend using external FPC dual-band antennas instead of PCB onboard antennas. The following are general instructions for PCB onboard antennas for reference only.

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

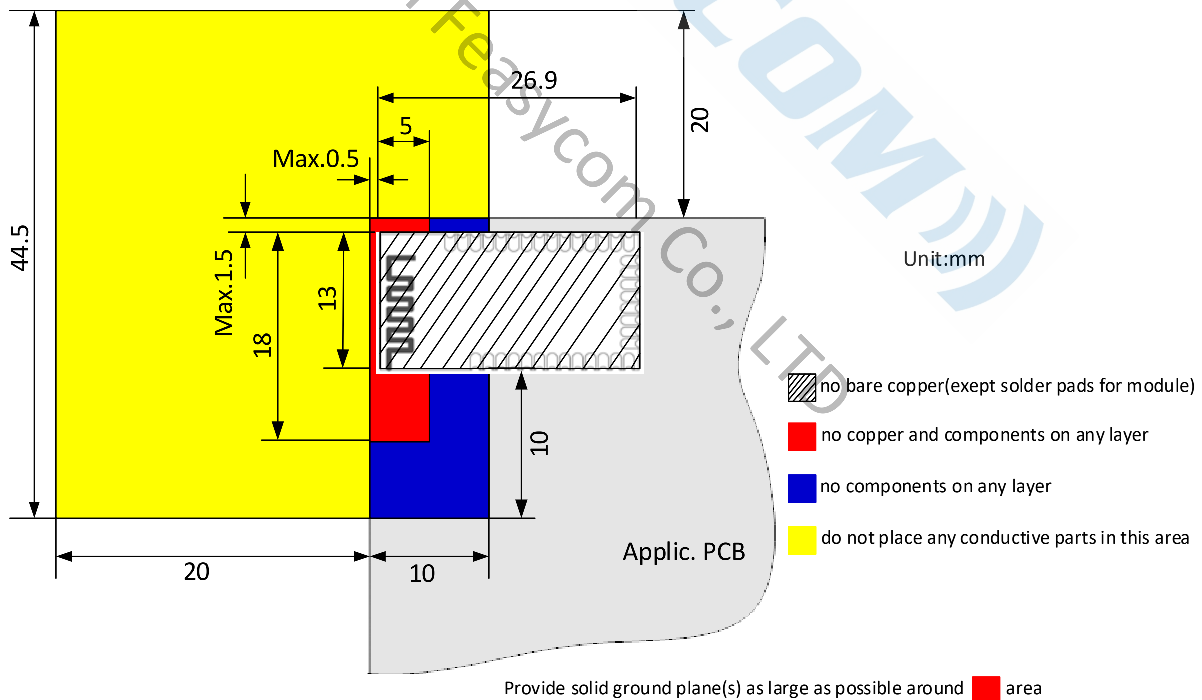

Figure 13-6：Restricted Area (Design schematic, for reference only.　Unit: mm)

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid

problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

13.7 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

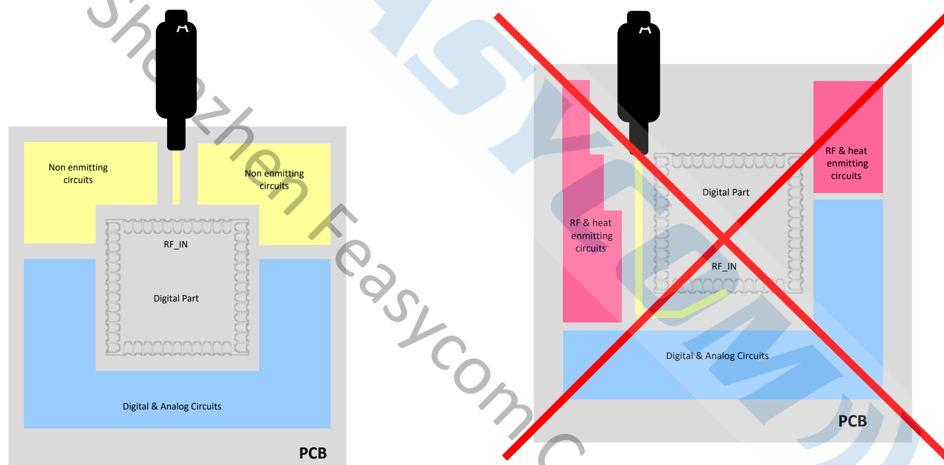

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Figure 13-7: Placement the Module on a System Board

13.7.1 Antenna Connection and Grounding Plane Design

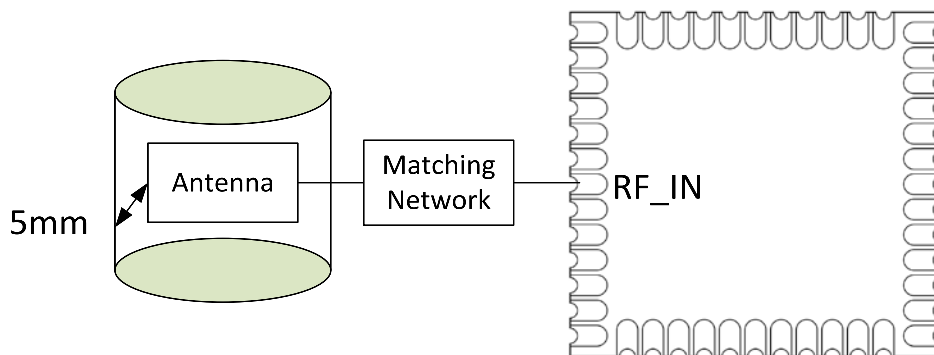

Figure 13-7-1: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

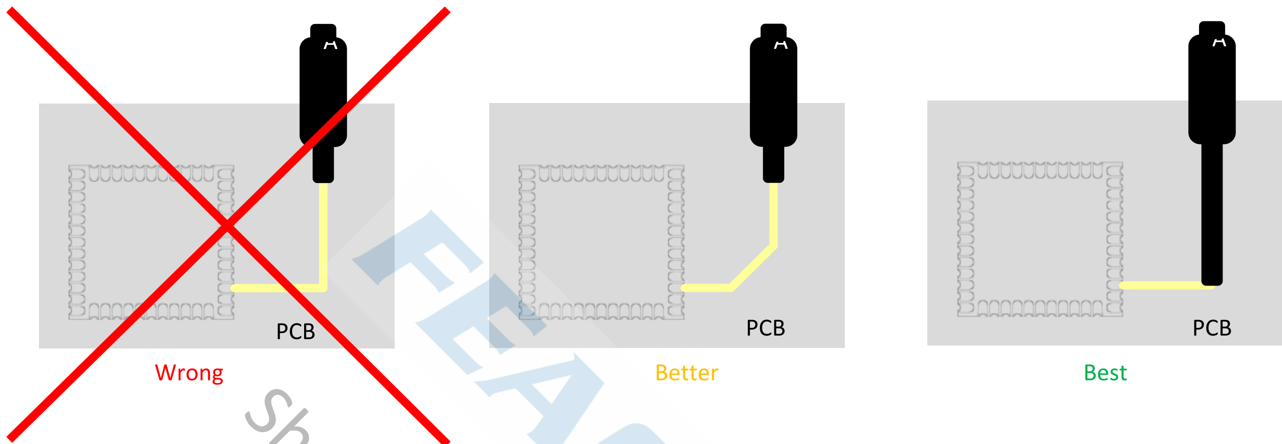

Figure 13-7-2: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

13.8 HCI Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 ~ 8mA

UART_RX

UART_TX

UART_CTS

UART_RTS

The route length of these signals be less than 15cm and the line impedance be less than 50Ω

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13.9 Power Trace Lines Layout Guideline

VDD_3V3 Trace Width: 40mil

VDDIO Trace Width: 20mil

13.10 Ground Lines Layout Guideline

A Complete Ground in Ground Layer.

Add Ground Through Holes to FSC-BW1501UV Module Ground Pads

Decoupling Capacitors close to FSC-BW1501UV Module Power and Ground Pads

14 PRODUCT PACKAGING INFORMATION

14.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 160mm * 310mm

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Figure 14-1: Tray vacuum

14.2 Packing box (Optional)

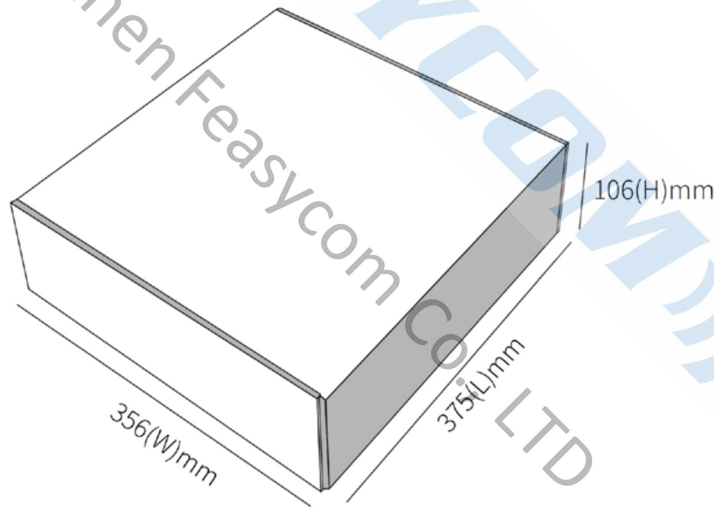

Figure 14-2: Packing box(Optional)

** If other packing is required, please confirm with the customer*

** Packing: 1000pcs per carton (Minimum packing quantity)*

** The outer packing size is for reference only, please refer to the actual size*

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15 APPLICATION SCHEMATIC