FSC-BW1001UV

DATASHEET V1.0

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Revision History

Version	Data	Notes	Author
V1.0	2024-09-21	Initial Version	Zoe

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1 INTRODUCTION

Overview

FSC-BW1001UV module integrates WLAN、BT/BLE in a single package module which support 802.11ax Wi-Fi 6Eand Bluetooth (BT) v5.3. The Module is based on QCA6688 chipset of Qualcomm, the module which uses the 112pins (around 76pins, bottom pads 36pins) 23mm*23mm LGA package and it can be used for high-speed wireless connectivity of automotive information and entertainment systems.

WLAN Features

- Supports 802.1la/b/g/n/ac/ax wi-Fi6e compliant;
- Supports 2x2 Multi-User Multiple-Input Multiple-Output (MU-MIMO)
- 20 MHz/40 MHz channel bandwidth for 2.4 GHz
- Dynamic Frequency Selection (DFS, radar detection)Offloading traffic for minimal host utilization at 11ac/ax speeds
- PCIE Gen 3
- Low-power PCIE (with L1 substate) interface
- Integrated close-loop power detector

Bluetooth Features

- Compliant with Bluetooth v5.3Supports LE Audio
- Supports 2 Mbps Bluetooth Low Energy (BLE), BLE long range
- Split ACL support for A2DP true stereo (earbuds)Dedicated Bluetooth antenna, sharing Bluetooth antenna with WLAN, and concurrent with 5G WLAN Dual eSCO/A2DP streams
- Supports class 1 and class 2 power-level transmissions without requiring an external power amplifier (PA)Backward-compatible with previous Bluetooth standards
- Flexible interface UART/PCM/I2S for Bluetooth audio

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2 General Specifications

Table 2-1： General Specifications

Categories	Features	Implementation
Bluetooth		
	Bluetooth Standard	Support Bluetooth 5.3
	Frequency Band	2.402GHz ~ 2.480GHz
	RF Input Impedance	50 ohms
	Interface	UART, PCM/I2S
	Antenna	External
	Support mode	Slave and Master
	Profiles	HFP/A2DP/AVRCP/PBAP/SPP/PAN/FTP/OPP/GATT/IAP2/ANCS/HID
	Maximum throughput	2,3Mbps
WLAN		
	Wi-Fi feature	2.4GHz: IEEE802.11 b/g/n radio 5GHz: IEEE802.11 a/n/ac/ax radio
	Frequency Band	2.4GHz /5GHz/6GHz
	RF Input Impedance	50 ohms
	Interface	PCIE
	Antenna	External
	Profiles	AP/Station/P2P
	Security	WAPI STA,WPA,WPA2,AES,TKIP,WPA3
operate condition		
	VDD_CORE_VL	0.95V
	VDD_CORE_VM	1.35V
	VDD_CORE_VH	1.9V
	VDD_PA	3.8V
	VDD18_IO	1.8V
	Temperature	-40°C to +85°C
	Humidity	10%~90% Non-Condensing
Dimension		
	Dimension	23mm(L)*23mm(W)*2.9mm(H)
ROHS		
	PCB Warpage	<0.5%(0.162mm)

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3 HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

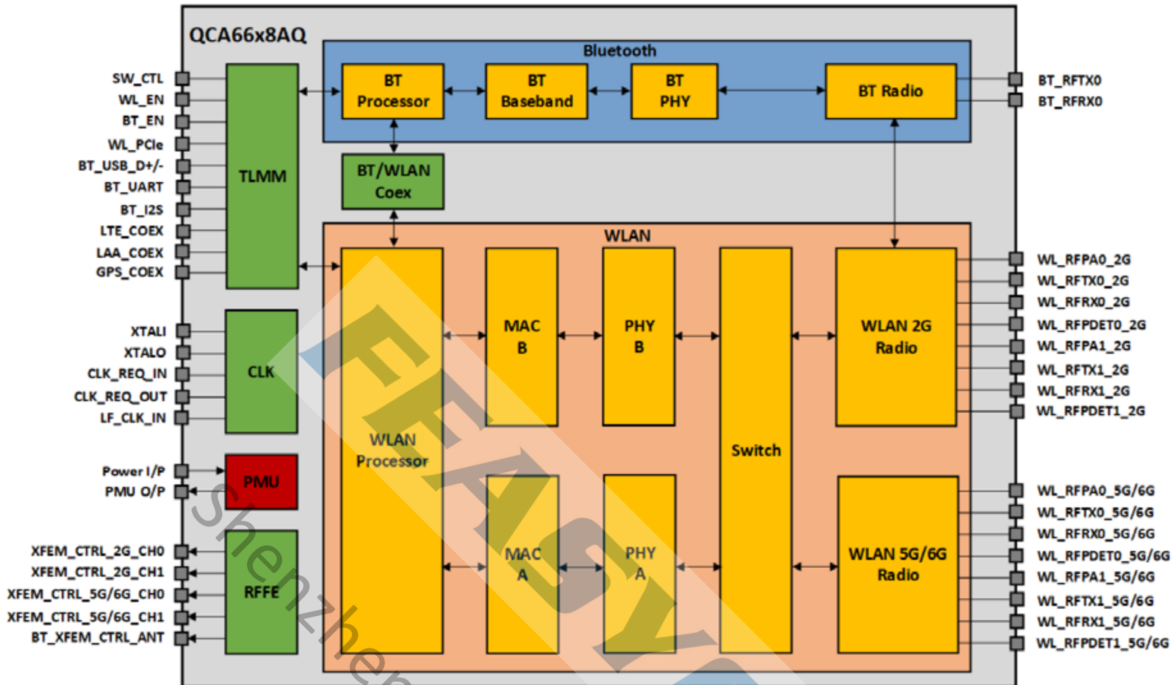

Figure 3-1-1: FSC-BW1001UV Block Diagram

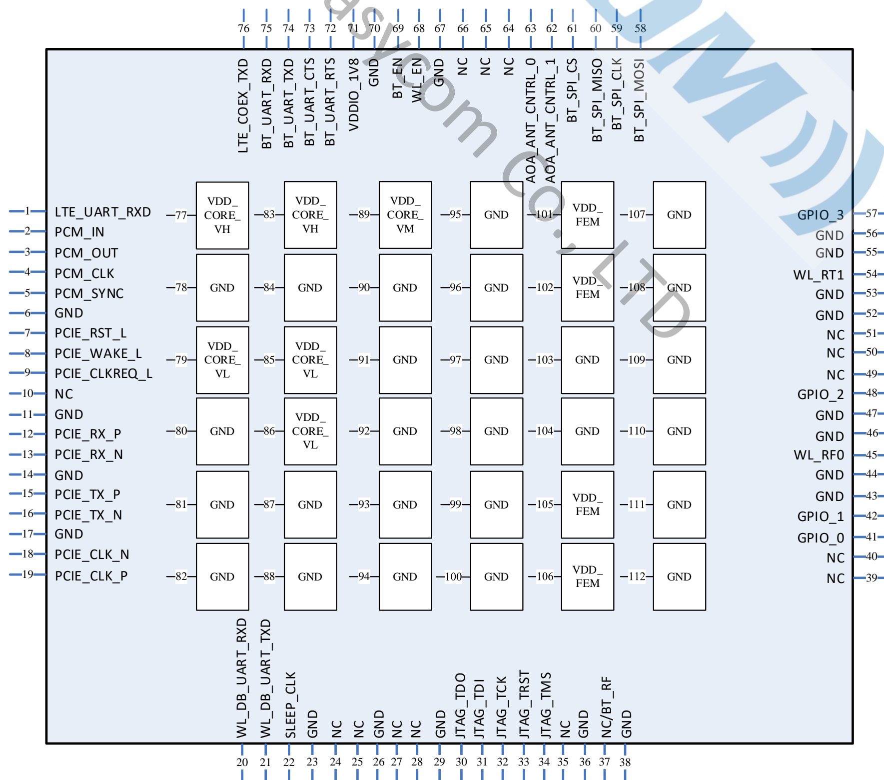

Figure 3-1-2: FSC-BW1001UV PIN Diagram (Top View)

3.2 PIN Definition Descriptions

Table 3-2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	LTE_COEX_RXD HOST_WAKE_BT	I	LTE co-existence /UART RX (default) Host wakes up Bluetooth (active high, used for 3rdparty host only)	
2	PCM_IN	I	Bluetooth PCM input signal (default)/I2S serial data input	
3	PCM_OUT	O	Bluetooth PCM output signal (default)/I2S serial data output	
4	PCM_CLK	I/O	Bluetooth PCM clock signal (default)/I2S serial clock	
5	PCM_SYNC	O	Bluetooth PCM synchronization signal(default) /I2S frame sync	
6	GND	GND	Ground	
7	PCIE_RST_L	I	WLAN PCIE reset signal is an input signal	
8	PCIE_WAKE_L	O	WLAN PCIE wake-up signal is an output signal. It is an open-drain signal that requires an external 10 KΩ pull-up resistor	
9	PCIE_CLKREQ_L	O	WLAN PCIE clock request signal is a bidirection signal. It is an open-drain signal that requires an external 10 KΩ pull-up resistor	
10	NC			
11	GND	GND	Ground	
12	PCIE_RX_P	I	PCIE Differential receive	
13	PCIE_RX_N	I	PCIE Differential receive	
14	GND	GND	Ground	
15	PCIE_TX_P	O	PCIE Differential transmit	
16	PCIE_TX_N	O	PCIE Differential transmit	
17	GND	GND	Ground	
18	PCIE_CLK_N	I	PCIE Differential reference clock	
19	PCIE_CLK_P	I	PCIE Differential reference clock	
20	WL_DB_UART_RXD	I	WLAN Debug UART Receive. It is an open drain signal and requires an external pull-up resistor if used	
21	WL_DB_UART_TXD	O	WLAN Debug UART Transmit. It is an open drain signal and requires an external pull-up resistor if used	
22	SLEEP_CLK	I	An external 32.768 KHz sleep clock input pin. A pull-down resistor is required if LF CLK IN is not used	
23	GND	GND	Ground	
24	NC			
25	NC			
26	GND	GND	Ground	
27	NC			
28	NC			
29	GND	GND	Ground	
30	JTAG_TDO	O	JTAG Test Data output	
31	JTAG_TDI	I	JTAG Test Data input	
32	JTAG_TCK	I	JTAG Test Clock	

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33	JTAG_TRST_N	I	JTAG Test Reset
34	JTAG_TMS	I	JTAG Test Mode Select
35	NC		
36	GND	GND	Ground
37	NC/BT_RF	NC/RF	NC/ Bluetooth RF output (Optional three-antenna configuration for dedicated Bluetooth RF I/O)
38	GND	GND	Ground
39	NC		
40	NC		
41	GPIO_0	I/O	Programmable GPIO Pin
42	GPIO_1	I/O	Programmable GPIO Pin
43	GND	GND	Ground
44	GND	GND	Ground
45	WL_RF0	RF	WLAN RF ANT0, includes 2G and 5G/6G WLAN
46	GND	GND	Ground
47	GND	GND	Ground
48	GPIO_2	I/O	Programmable GPIO Pin
49	NC		
50	NC		
51	NC		
52	GND	GND	GROUND
53	GND	GND	GROUND
54	WL_RF1	RF	WLAN RF ANT1, includes 2G and 5G/6G WLAN
55	GND	GND	Ground
56	GND	GND	Ground
57	GPIO_3	I/O	Programmable GPIO Pin
58	BT_SPI_MOSI	I	Bluetooth SPI Master Out Slave In
59	BT_SPI_CLK	I	Bluetooth SPI Clock
60	BT_SPI_MISO	O	Bluetooth SPI Maser In Slave Out
61	BT_SPI_CS	I	Bluetooth SPI Chip Select
62	AOA_ANT_CNTRL_1	-	For the external FEM control pin ,if not in use, please suspend the PIN
63	AOA_ANT_CNTRL_0	-	For the external FEM control pin ,if not in use, please suspend the PIN
64	NC		
65	NC		
66	NC		
67	GND	GND	Ground
68	WL_EN	I	WLAN enable signal. It is an input, active high to enable WLAN operation
69	BT_EN	I	Bluetooth enable signal. It is an input, active high to enable Bluetooth operation.
70	GND	GND	Ground

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71	VDDIO_1V8	PI	VDDIO input at 1.8V (50mA peak)
72	BT_UART_RTS	I	UART_RTS(connected to the UART_CTS of Host)
73	BT_UART_CTS	O	UART_CTS(connected to the UART_RTS of Host)
74	BT_UART_TXD	O	UART_TXD(connected to the UART_RXD of Host)
75	BT_UART_RXD	I	UART_RXD(connected to the UART_TXD of Host)
76	LTE_COEX_TXD BT_WAKE_HOST	O	LTE co-existence UART TX(default) Bluetooth wakes up Host (active high, used for 3rdparty host only)
77、83	VDD_CORE_VH	PI	Voltage for Core, high voltage; 1.95V supply
79、85、86	VDD_CORE_VL	PI	Voltage for Core, low voltage; 0.95V supply
89	VDD_CORE_VM	PI	Voltage for Core, mid voltage; 1.35V supply
101、102、105、106	VDD_FEM	PI	Voltage for PA in module; 3.85V supply
78、80~82、84、87~88、90~100 、103~104 、107~112	Thermal pad	GND	GROUND

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4 ELECTRICAL CHARACTERISTICS

4.1 Max Range

Table 4-1：Max Range

Parameter	Min	Type	Max	Unit
VDD_CORE_VL	-0.3		2.1	V
VDD_CORE_VM	-0.3		1.55	V
VDD_CORE_VH	-0.3		2.15	V
VDDIO_18	-0.3		1.89	V
VDD_FEM	-0.3		2.2	
Operating temperature range	-40		+85	° C
Storage temperature range	-40		+125	° C
ESD Stress Voltage To be updated after the completion of QUAL	-2000		+2000	V

4.2 General Requirements and Operation

Table 4-2-1：General Requirements and Operation

Parameter	Sym	Type	Unit
VDD_CORE_VL	VBAT	0.95	V
VDD_CORE_VM	VIO	1.35	V
VDD_CORE_VH		1.90	V
VDDIO_18		1.80	V
VDD_FEM		1.8	V

5 Standard test condition

5.1 Standard condition

Temperature： In a range of +23℃±5℃

6 Module RF Performances

6.1 WLAN Performances

6.1.1 WLAN 2.4GHz Receiver Characteristics

Table 6-1-1： WLAN 2.4GHz Receiver Characteristics

Parameter	Mode	Data rate	Modulation	Std	Unit
Frequency Range				2.4-2.496	GHz
RX Sensitivity	802.11b	1Mbps	CCK	-99	dBm
	802.11b	11Mbps	CCK	-91.5	dBm
	802.11g	6 Mbps	BPSK	-96	dBm
		54 Mbps	QAM64	-77.5	dBm
	802.11n HT20 802.11ac VHT20	MCS0	BPSK	-95	dBm
		MCS7	QAM64	-75	dBm
		MCS8	QAM12	-74.5	dBm
	802.11n HT40 802.11ac VHT40	MCS0	BPSK	-93	dBm
		MCS7	QAM64	-72.5	dBm
		MCS9	QAM256	-69.5	dBm
	802.11ax HE20	MCS0	BPSK	-95	dBm
		MCS7	QAM64	-74	dBm
		MCS9	QAM256	-70.5	dBm
		MCS11	QAM1024	-65	dBm
		MCS13	QAM4096	-58	dBm
	802.11ax HE40	MCS0	BPSK	-93	dBm
		MCS7	QAM64	-72	dBm
		MCS9	QAM256	-68.5	dBm
		MCS11	QAM1024	-63	dBm
		MCS13	QAM4096	-56	dBm

6.1.2 WLAN 2.4GHz Transmitter Power

Table 6-1-2： WLAN 2.4GHz Transmitter Power

Parameter	Mode	Data rate	Modulation	Std	Unit
Frequency Range				2.4-2.496	GHz
TX output Power	802.11b	1Mbps	CCK	22	dBm

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	802.11b	11Mbps	CCK	22	dBm
	802.11g	6 Mbps	BPSK	21	dBm
		54 Mbps	QAM64	20	dBm
	802.11n HT20 802.11ac VHT20	MCS0	BPSK	21	dBm
		MCS7	QAM64	19	dBm
		MCS9	QAM256	18.5	dBm
	802.11n HT40 802.11ac VHT40	MCS0	BPSK	21	dBm
		MCS7	QAM64	18.5	dBm
		MCS9	QAM256	17.5	dBm
	802.11ax HE20	MCS0	BPSK	21	dBm
		MCS7	QAM64	18.5	dBm
		MCS9	QAM256	17.5	dBm
		MCS11	QAM1024	16.5	dBm
		MCS13	QAM4096	15	dBm
	802.11ax HE40	MCS0	BPSK	20.5	dBm
		MCS7	QAM64	18	dBm
		MCS9	QAM256	17	dBm
		MCS11	QAM1024	16	dBm
		MCS13	QAM4096	14.5	dBm

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6.2 WLAN 5 GHz Radio Characteristics

6.2.1 WLAN 5 GHz Rx RF Characteristics

Table 6-2-1：WLAN 5 GHz Rx RF Characteristics

Parameter	Mode	Data rate	Modulation	Std	Unit
Frequency Range				4.9-7.125	GHz
RX Sensitivity	802.11a	6 Mbps	BPSK	-97	dBm
		54 Mbps	QAM64	-79.5	dBm
	802.11n HT20	MCS0	BPSK	-96.5	dBm
		MCS7	QAM64	-79	dBm
	802.11n HT40	MCS0	BPSK	-94	dBm
		MCS7	QAM64	-76.5	dBm
	802.11ac VHT20	MCS0	BPSK	-96.5	dBm
		MCS9	QAM256	-75	dBm
	802.11ac VHT40	MCS0	BPSK	-94	dBm
		MCS9	QAM256	-69.5	dBm
	802.11ac VHT80	MCS0	BPSK	-91.5	dBm
		MCS9	QAM256	-67	dBm

	802.11ax HE20	MCS0	BPSK	-97	dBm
		MCS11	QAM1024	-66	dBm
	802.11ax HE40	MCS0	BPSK	-94	dBm
		MCS11	QAM1024	-64	dBm
	802.11ax HE80	MCS0	BPSK	-91	dBm
		MCS11	QAM1024	-60.5	dBm
		MCS13	QAM4096	-53.5	dBm
	802.11ax HE160	MCS0	BPSK	-88	dBm
		MCS11	QAM1024	-58.5	dBm
		MCS13	QAM4096	-51.5	dBm

6.2.2 WLAN 5 GHz Transmitter Power

Table 6-2-2： WLAN 5 GHz Transmitter Power

Parameter	Mode	Data rate	Modulation	Std	Unit
Frequency Range				4.9-7.125	GHz
TX output Power	802.11a	6 Mbps	BPSK	21	dBm
		54 Mbps	QAM64	18.5	dBm
	802.11n HT20	MCS0	BPSK	21	dBm
		MCS7	QAM64	18	dBm
	802.11n HT40	MCS0	BPSK	20.5	dBm
		MCS7	QAM64	17.5	dBm
	802.11ac VHT20	MCS0	BPSK	21	dBm
		MCS9	QAM256	18	dBm
	802.11ac VHT40	MCS0	BPSK	20.5	dBm
		MCS9	QAM256	17.5	dBm
	802.11ac VHT80	MCS0	BPSK	19.5	dBm
		MCS9	QAM256	15	dBm
	802.11ax HE20	MCS0	BPSK	21	dBm
		MCS11	QAM1024	14	dBm
	802.11ax HE40	MCS0	BPSK	20.5	dBm
		MCS11	QAM1024	13.5	dBm
	802.11ax HE80	MCS0	BPSK	20	dBm
		MCS11	QAM1024	13	dBm
		MCS13	QAM4096	11	dBm
	802.11ax HE160	MCS0	BPSK	19.5	dBm
		MCS11	QAM1024	12.5	dBm
		MCS13	QAM4096	10.5	dBm

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6.3 WLAN 6 GHz Radio Characteristics

6.3.1 WLAN 6 GHz Rx RF Characteristics

Table 6-3-1: WLAN 6 GHz Rx RF Characteristics

Parameter	Mode	Data rate	Modulation	Std	Unit
Frequency Range				4.9-7.125	GHz
RX Sensitivity	802.11a	6 Mbps	BPSK	-95	dBm
		54 Mbps	QAM64	-77.5	dBm
	802.11ac VHT20	MCS0	BPSK	-94.5	dBm
		MCS9	QAM256	-73	dBm
	802.11ac VHT40	MCS0	BPSK	-92	dBm
		MCS9	QAM256	-67.5	dBm
	802.11ac VHT80	MCS0	BPSK	-89.5	dBm
		MCS9	QAM256	-65	dBm
	802.11ax HE20	MCS0	BPSK	-95	dBm
		MCS11	QAM1024	-64	dBm
	802.11ax HE40	MCS0	BPSK	-92	dBm
		MCS11	QAM1024	-62	dBm
	802.11ax HE80	MCS0	BPSK	-89	dBm
		MCS11	QAM1024	-58.5	dBm
		MCS13	QAM4096	-51.5	dBm
	802.11ax HE160	MCS0	BPSK	-86	dBm
		MCS11	QAM1024	-56.5	dBm
		MCS13	QAM4096	-49.5	dBm

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6.3.2 WLAN 6 GHz Transmitter Power

Table 6-3-2: WLAN 6 GHz Transmitter Power

Parameter	Mode	Data rate	Modulation	Std	Unit
Frequency Range				-	-
TX output Power	802.11a	6 Mbps	BPSK	20	dBm
		54 Mbps	QAM64	17.5	dBm
	802.11ax HE20	MCS0	BPSK	20	dBm
		MCS11	QAM1024	13	dBm
	802.11ax HE40	MCS0	BPSK	19.5	dBm
		MCS11	QAM1024	12.5	dBm
	802.11ax HE80	MCS0	BPSK	19	dBm
		MCS11	QAM1024	12	dBm
		MCS13	QAM4096	10	dBm

	802.11ax HE160	MCS0	BPSK	18.5	dBm
		MCS11	QAM1024	11.5	dBm
		MCS13	QAM4096	9.5	dBm

6.4 BT Performance

6.4.1 BT Performance

Table 6-4-1: BT Performance

Parameter		Condition	Std	Unit
Test frequency range		2402 to 2480	-	MHz
Step size of Power Control		Channel 0 Channel 39 Channel 78	2～8	dB dB dB
ICFT (Initial Carrier Frequency Tolerance)		Channel 0 Channel 39 Channel 78	-75～75	KHz KHz KHz
Output Power		Channel 0 Channel 39 Channel 78	TBD	dBm dBm dBm
Carrier Frequency Drift	Channel: 0	DH1 DH1 Drift rata/50us DH3 DH3 Drift rata/50us DH5 DH5 Drift rata/50us	25~-25 -20～20 -40～40 -20～20 -40～40 -20～20	KHz KHz KHz KHz KHz KHz
	Channel: 39	DH1 DH1 Drift rata/50us DH3 DH3 Drift rata/50us DH5 DH5 Drift rata/50us	-25～25 -20～20 -40～40 -20～20 -40～40 -20～20	KHz KHz KHz KHz KHz KHz
	Channel: 78	DH1 DH1 Drift rata/50us DH3 DH3 Drift rata/50us DH5 DH5 Drift rata/50us	-25～25 -20～20 -40～40 -20～20 -40～40 -25～25	KHz KHz KHz KHz KHz KHz

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Modulation characteristic	Channel: 0	Df1avg Df2avg Df2avg/Df1avg	140～175 ⩾115 ⩾0.8	KHz KHz
	Channel: 39	Df1avg Df2avg Df2avg/Df1avg	140～175 ⩾115 ⩾0.8	KHz KHz
	Channel: 78	Df1avg Df2avg Df2avg/Df1avg	140～175 ⩾115 ⩾0.8	KHz KHz
Sensitivity (single/ multi slot packets) （Power=-70dBm)		Channel 0 Channel 39 Channel 78	BER ⩽ 0.1% BER ⩽ 0.1% BER ⩽ 0.1%	
Maximum input Level （Power=-20dBm)		Channel 0 Channel 39 Channel 78	BER ⩽ 0.1% BER ⩽ 0.1% BER ⩽ 0.1%	

6.4.2 BT EDR Performance

Table 6-4-2：BT EDR Performance

Parameter		Condition	Std	Unit
Test frequency range		2402 to 2480	-	MHz
EDR relative power	Channel: 0 Channel: 39 Channel: 78	PGFSK PDPSK PGFSK PDPSK PGFSK PDPSK	－4dB < PDPSK- PGFSK < + 1dB	dB dB dB dB dB dB
EDR carry frequency accuracy and modulation accuracy	Channel: 0 Channel: 39 Channel: 78	RMS DEVM(EDR2) RMS DEVM(EDR3) 99% DEVM(EDR2) 99% DEVM(EDR3) Peak DEVM(EDR2) Peak DEVM(EDR3)	< 0.2 < 0.13 < 0.3 < 0.2 < 0.35 < 0.25	
Sensitivity (Power=-70dBm)	Channel: 0 Channel: 39 Channel: 78	EDR2 EDR3	BER⩽0.1% BER⩽0.1%	
Maximum input Level (Power=-20dBm)	Channel: 0 Channel: 39 Channel: 78	EDR2 EDR3	BER⩽0.1% BER⩽0.1%	

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6.4.3 BT BLE Performance

Table 6-4-3: BT BLE Performance

Parameter		Condition	Std	Unit
Test frequency range		2402 to 2480	-	MHz
ICFT (Initial Carrier Frequency Tolerance)		Channel: 0 Channel: 19 Channel: 39	-100～100	KHz KHz KHz
Output Power		Channel: 0 Channel: 19 Channel: 39	TBD	dBm dBm dBm
Carrier Frequency Drift		Channel: 0 Channel: 19 Channel: 39	-25~25	KHz KHz KHz
Modulation characteristic	Channel: 0	Df1avg Df2avg Df2avg/Df1avg	225～275 ≥185 ≥0.8	KHz KHz
	Channel:19	Df1avg Df2avg Df2avg/Df1avg	225～275 ≥185 ≥0.8	KHz KHz
	Channel: 39	Df1avg Df2avg Df2avg/Df1avg	225～275 ≥185 ≥0.8	KHz KHz
Sensitivity (Power=-70dBm)	Channel: 0 Channel: 19 Channel: 39	Power=-70dBm Power=-70dBm Power=-70dBm	BER≤0.1% BER≤0.1% BER≤0.1%	
Maximum input Level (Power=-20dBm)	Channel: 0 Channel: 19 Channel: 39	Power=-70dBm Power=-70dBm Power=-70dBm	BER≤0.1% BER≤0.1% BER≤0.1%	

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7 Reliability Test

7.1 Item of Reliability Test

Table 7-1: Item of Reliability Test

Test Item	Specification
High Temperature(Storage)	Place 96 hours at 90°C environment, and 2 hours at normal temperature and humidity then test, module should meet the standard of chapter 7.2
Low Temperature(Storage)	Place 96 hours at 90°C environment, and 2 hours at normal temperature and humidity then test, module should meet the standard of chapter 7.2
High Humidity(Storage)	At the temperature of +60°C, 90%RH environment for 96 hours, and 2 hours at normal temperature and humidity, then test, module should meet the standard of chapter 7.2.

High Temperature(Operating)	At the temperature of +60°C, 90%RH environment for 96 hours, and 2 hours at normal temperature and humidity, then test, module should meet the standard of chapter 7.2.
Low Temperature(Operating)	Module must be able to work continuously for 96 hours at t the environment of -40°C , The module should work normal within the time or module should meet the standard of chapter 7.2 .
High and low temperature cycling test	Tstg Max 85°C 30 min s, Temperature shift time: within 2hrs. Tstg Min -40°C 30 min, Repeat 10 cycles. The module should be cold to normal temperature for two hours, module should meet the standard of chapter 7.2
Vibration Resistance	Freq: 10~200Hz, 0.1 oct/min, max acceleration: 2.5Grms-Test time: X, Y, Z axis for 6 hours. After 1 hour vibration test, do the test in each direction. In normal temperature condition, take measurements within 3 hours. Module should meet the standard of chapter 7.2
Shock Test	Shock Test: Impact acceleration: 70G(m/sec2), impact time: 11 ms, impact frequency and direction: 10 times each in 6 directions. In normal temperature condition, take measurements within 3hr， Module should meet the standard of chapter 7.2

7.2 Reliability Test Standard

Table 7-2-1：WLAN 2.4G Performance

Item	Condition	mode	rate	Unit	Std
Transmitter Power	@2412/2437/2462MHz	DSSS CCK	11Mbps 54Mbps	dBm dBm	10~20 6~20
EVM	@2412/2437/2462MHz	DSSS	1Mbps 54Mbps	dB dB	≦-10 ≦-25
Receiver sensitivity	At < 10% PER limit @2412/2437/2462MHz	11b mode： DSSS （PER<8%） 11g mode： OFDM （PER<10%）	11Mbps 54Mbps	dBm dBm	≦-82 ≦-65

Table 7-2-2：WLAN 5G Performance

Item	Condition	mode	rate	Unit	Std
Transmitter Power	@5210/5530/5745MHz	11ac OFDM	MCS9	dBm	4~20
EVM	@5210/5530/5745MHz	11ac OFDM	MCS9	dB	≦-32
Receiver sensitivity	@5210/5530/5745MHz	11ac OFDM	MCS9	dBm	≦-51

Table 7-2-3：BT Performance

Parameter	Condition	Std	Unit
Test frequency	2402(Channel0) 2441(Channel39) 2480(Channel78)		MHz
BR Output Power		-6～20	dBm
single/ multi slot packets Sensitivity (Power=-70dBm)	Power-70dBm	BER≤ 0.1%	

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8 PHYSICAL INTERFACE

8.1 HCI UART INTERFACE

Table 8-1-1: UART Parameters

Parameter	Value
Number of data bits	Eight
Parity bit	No parity
Stop bit	One stop bit
Flow control	RTS/CTS (hardware)
Flow off response	Two bytes maximum
Supported transport bit rates (bps) [a]	9.6 K, 19.2 K, 38.4 K, 57.6 K, 115.2 K, 125 K, 230.4 K, 250 K, 460.8 K, 500 K, 720 K, 921.6 K, 1 M, 1.6 M, 2 M, 3 M, 3.2 M, with an accuracy of +1.5/-2.5%

[a] UART maximum baud rate is 3.2 Mbps.

The HCI UART transmit timing is shown in the following figure and table.

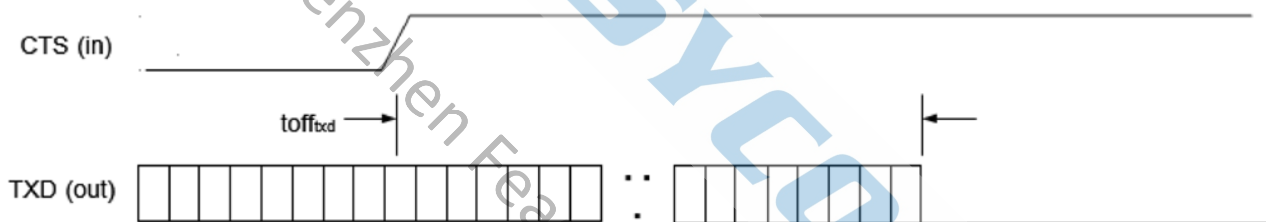

Figure 8-1-1: HCI UART transmit flow control timing

Table 8-1-2: HCI UART transmit flow control timing

Parameter	Description	Min.	Typ.	Max.	Unit
$toff_{txd}$	Delay from CTS to TXD stop			1	byte

The HCI UART receive timing is shown in the following figure and table.

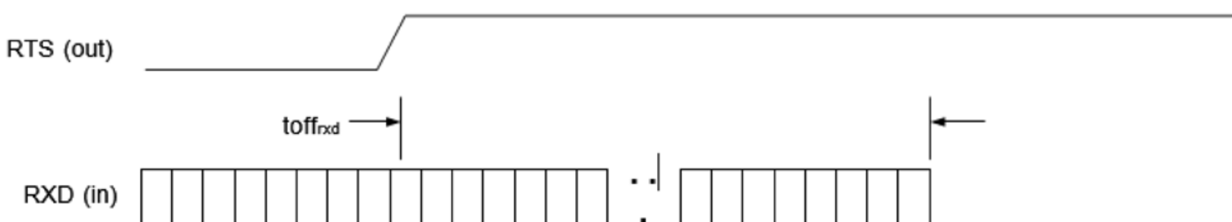

Figure 8-1-2: HCI UART receive flow control timing

Table 8-1-3: HCI UART receive flow control timing

Parameter	Description	Min.	Typ.	Max.	Unit
$toff_{txd}$	Delay from RTS to RXD stop	16			byte

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8.2 Bluetooth PCM interface

The pulse coded modulation (PCM) interface connects the QCA6688AQ device to the phone's audio interface, or to peripheral devices, such as a codec. The PCM interface circuits use digital l/0 pins that receive power from the VDD I/O supply. The QCA6688AQ PCM interface has been designed to minimize audio latency.

The following table lists the typical audio latencies for various packet types.

Table 8-2-1：Typical PCM interface audio latency

Packet type	Audio latency
HV3/EV3 T_{eSCO} = 6, W_{eSCO} = 0	4.4 ms
EV3 T_{eSCO} = 6, W_{eSCO} = 2	5.7 ms
EV3 T_{eSCO} = 6, W_{eSCO} = 4	6.9 ms

The PCM interface is configured to operate as master or slave. In each case, the PCM_IN pin is the data receive terminal (an input), and the PCM_OUT pin is the data transmit terminal (an output). The clock and sync pins function as inputs or outputs, depending on whether the QCA6688AQ PCM interface is configured as a master or slave:

- When the QCA6688AQ PCM interface is the master: PCM_CLK and PCM_SYNC are outputs from the QCA6688AQ to the PCM bus slave(s).
- When the QCA6688AQ PCM interface is the slave: PCM_CLK and PCM_SYNC are inputs to the QCA6688AQ device from the PCM bus master.

The following table lists the PCM interface specifications:

Table 8-2-2：PCM interface specifications

Parameter	Description	Min.	Typ.	Max.	Unit
Clock rate (slave)	Determined by the master	64		2,048	kHz
Clock rate (master)		64		2,048	kHz
Frame size		1	8	256	Bits
Slot size		1	13	16	Bits
Slot number	Number of slots that can be configured per frame	1		32	Slots/frame

Example timing diagrams and specifications for slave and master configurations are described in the following tables and illustrations. (32 MHz*N/4,000), in which N is an integer, $8 \leqslant N \leqslant 256$

:

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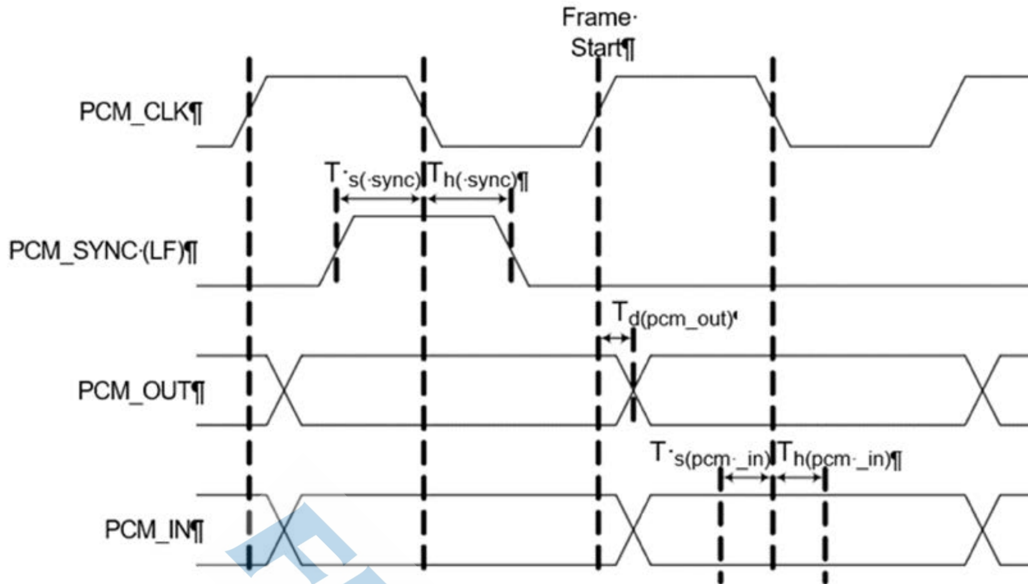

Figure 8-2-1: PCM interface timing diagram (slave)

Table 8-2-3: PCM interface timing in slave mode

Symbol	Description	Min.	Typ.	Max.	Unit
F_{pcm_clk}	PCM_CLK frequency	64		2,048	kHz
Ts_{pcm_sync}	Setup time PCM_SYNC to PCM_CLK fall	0			ns
Th_{pcm_sync}	Hold time PCM_CLK fall to PCM_SYNC fall	150			ns
Td_{pcm_out}	Delay from PCM_CLK rise to PCM_OUT	0		150	ns
Ts_{pcm_in}	Setup time PCM_IN to PCM_CLK fall	0			ns
Th_{pcm_in}	Hold time PCM_IN after PCM_CLK fall	150			ns

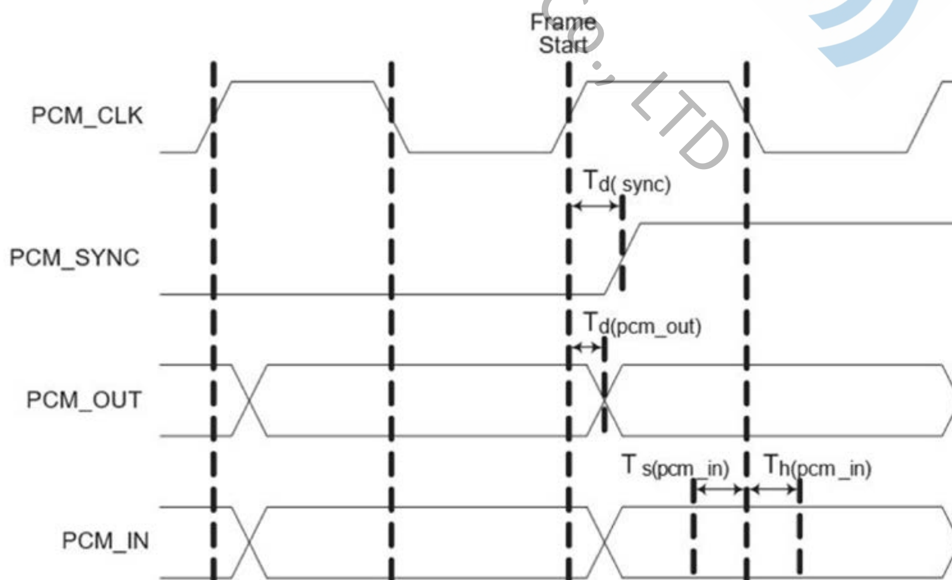

Figure 8-2-2: PCM interface timing diagram (master)

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Table 8-2-4: PCM interface timing in slave mode

Symbol	Description	Min.	Typ.	Max.	Unit
F_{pcm_clk}	PCM_CLK frequency	64		2048	kHz
Ts_{pcm_sync}	Delay from PCM_CLK rise to long SYNC	-10		50	ns
Td_{pcm_out}	Delay from PCM_CLK rise to PCM_OUT	-10		50	ns
Ts_{pcm_in}	Setup time PCM_IN to PCM_CLK fall	50			ns
Th_{pcm_in}	Hold time PCM_IN after PCM_CLK fall	150			ns

9 MSL & ESD

Table 9-1: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade	Electrostatic discharge
ESD – Human Body Model (HBM) Rating JESD22-A114-B	Pass ±2000 V, all pins
ESD – Charged Device Model (CDM) Rating JESD22-C101-D	Pass ±250 V, all pins

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10 RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to reflow, it is crucial to ensure that the modules are properly packaged to prevent moisture absorption. The new packages are equipped with desiccants to absorb moisture, and a humidity indicator card is included to indicate the moisture level maintained during storage and shipment. If the card indicates the need to bake the units, please refer to the instructions specified by IPC/JEDEC J-STD-033 and follow them accordingly. It is important to adhere to these instructions to prevent any potential moisture-related issues during the reflow process.

Note: The shipping tray should not be exposed to temperatures exceeding 65°C. If baking is necessary at higher temperatures indicated below, it is essential to remove the modules from the shipping tray. This precaution is important to avoid any potential damage or deformation to the tray caused by excessive heat.

Any module that exceeds its floor life but has not yet been manufactured should be repackaged by using new desiccants and humidity indicator cards. For devices with a Moisture Sensitivity Level (MSL) of 3, the floor life is 168 hours in an environment with 30°C/60%RH.

Floor life refers to the maximum allowable time a moisture-sensitive device can be exposed to ambient conditions without risking moisture absorption and potential damage during soldering.

Notice (注意):

When using our modules, it is recommended to use a step steel mesh with a thickness of 0.16-0.20mm. However, the thickness can be adjusted according to the adaptability of your own product.

使用我司模块，须使用阶梯钢网，建议阶梯钢网厚度0.16-0.20mm，可根据自己产品适应性，进行相应调整.

Table 10-1-1 Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to simplify manufacturing processes, such as reflow soldering on a PCB. However, Customers are responsible for selecting the appropriate solder paste and confirming that the oven temperatures during reflow meet with the specifications provided by the solder paste manufacturer. Notably, Feasycom surface mount modules adhere to the J-STD-020D1 standards for reflow temperatures.

The soldering profile may vary depending on different parameters, requiring a specific setup for each application. The data provided here is only intended as a general guideline for solder reflow and should be used as a reference.

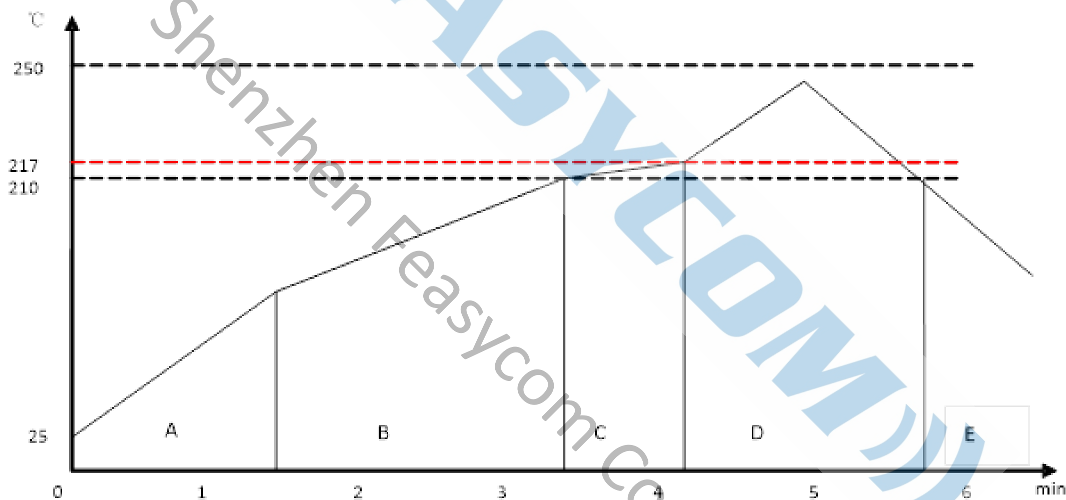

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Figure 10-1-1：Typical Lead-free Re-flow

Pre-heat zone (A) — This zone gradually increases the temperature at a controlled rate, usually **ranging from 0.5 to 2 °C/s**. Its purpose is to preheat the PCB board and components to a temperature of 120-150 °C. This stage is necessary to ensure the even distribution of heat across the PCB board and to remove any remaining solvents completely, minimizing the risk of heat shock to the components.

Equilibrium Zone 1 (B) — In this stage, the flux undergoes softening and uniformly covers the solder particles, as well as spreading over the PCB board. This process helps prevent re-oxidation of the solder particles. Additionally, as the temperature rises and the flux liquefies, each activator and rosin component become activated. They work together to eliminate any oxide film formed on the surface of the solder particles and PCB board. **For this zone, it is recommended to maintain a temperature range of 150 to 210 °C for a duration of 60 to 120 seconds.**

Equilibrium Zone 2 (C) (optional) — To address the issue of upright components, it is recommended to maintain a temperature range of 210 to 217 °C for a duration of approximately 20 to 30 seconds. This will help ensure proper soldering and alignment of the components on the PCB board.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-

free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

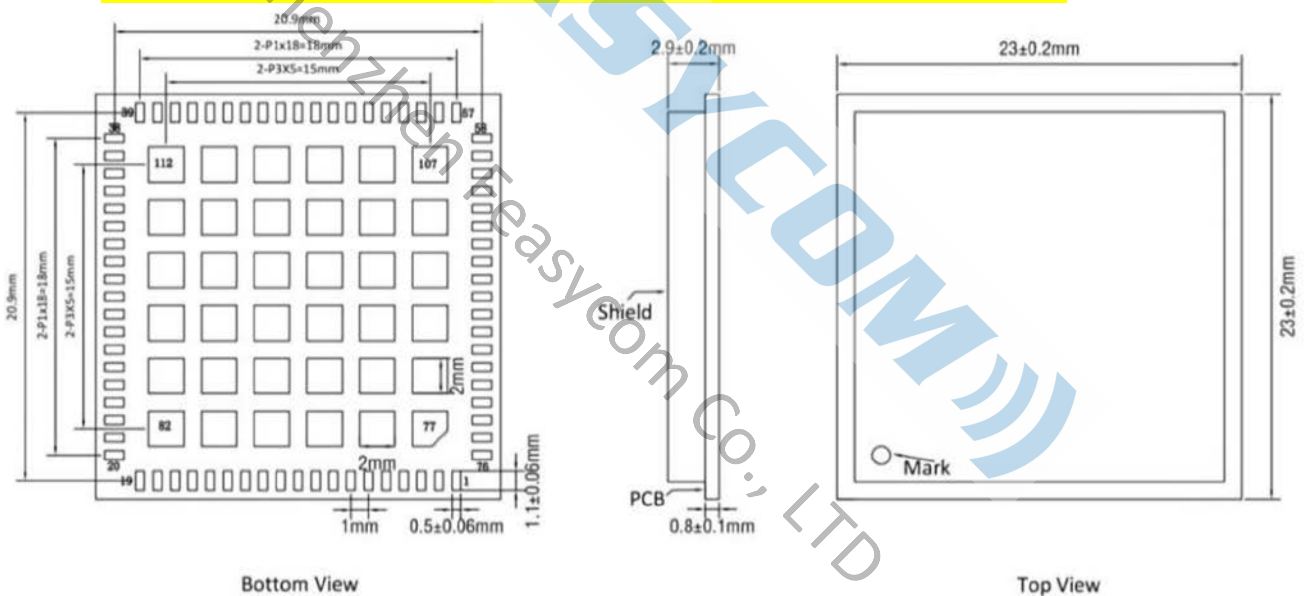
Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

11 MECHANICAL DETAILS

11.1 Mechanical Details

- Dimension: 23mm(W) x 23mm(L) x 2.9mm(H) Tolerance: ±0.2mm
- Module size: 23mm X 23mm Tolerance: ±0.2mm
- Pad size: 1.1mm X 0.5mm,2.0mm X 2.0mm Tolerance: ±0.1mm
- Pad pitch: 1.0mm Tolerance: ±0.1mm

(分板后边角残留板边误差：不大于 0.5mm) (Residual plate edge error: < 0.5mm)



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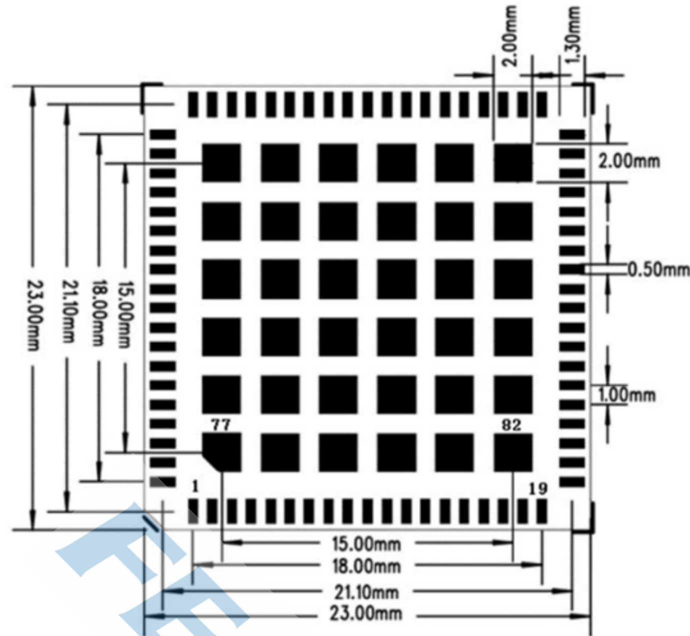

Figure 11-1-1：FSC-BW1001UV footprint Layout Guide (Top View)

12 HARDWARE INTEGRATION SUGGESTIONS

12.1 Connections when BT's HCI is by UART

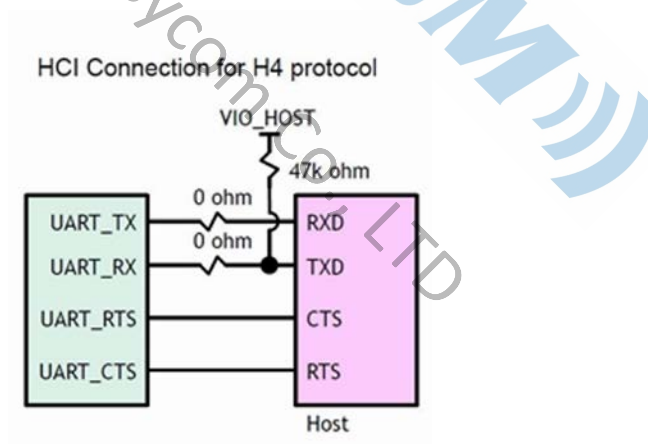

Figure 12-1-1: Connections when BT's HCI is by UART

Note:

1. Reserve a 47k pull-high resistor on host TXD when this port is not in output mode for default.

   (If not sure, reserve a 47k resistor is recommended for avoid TXD being floating)

2. There must be 0 ohm jumper-resistors on TX/RX paths, for BQB certification test.

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12.2 RF Circuit- RF pads

- Some RF components such as 0402-packaged RLC, connectors, or module pins are with large soldering pad, those pads have higher parasitic capacitance which can impact the characteristic impedance of RF traces.
- The GND under those pads shall be dug out, shown as below, for keeping good 50Ω matching.
- The dig-out layers and area should be calculated carefully, we recommend digging the area a little higher than the simulation results.

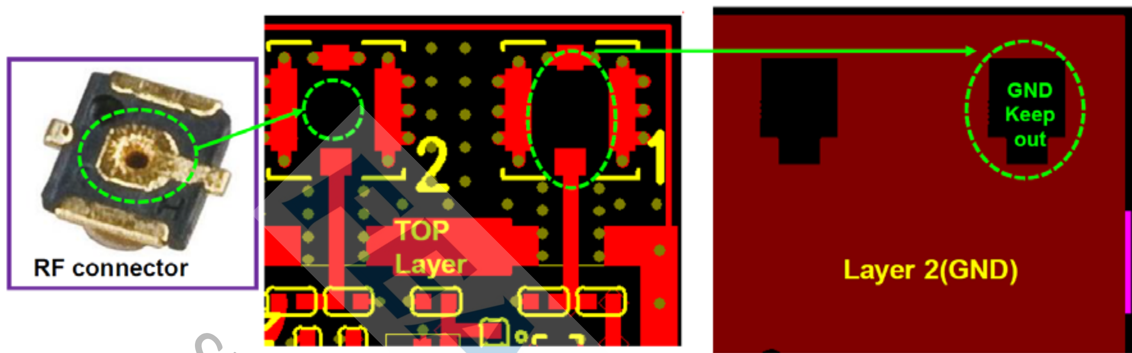

Figure 12-2-1: RF Circuit- RF pads

12.3 Recommendable antenna & IPEX by Feasycom

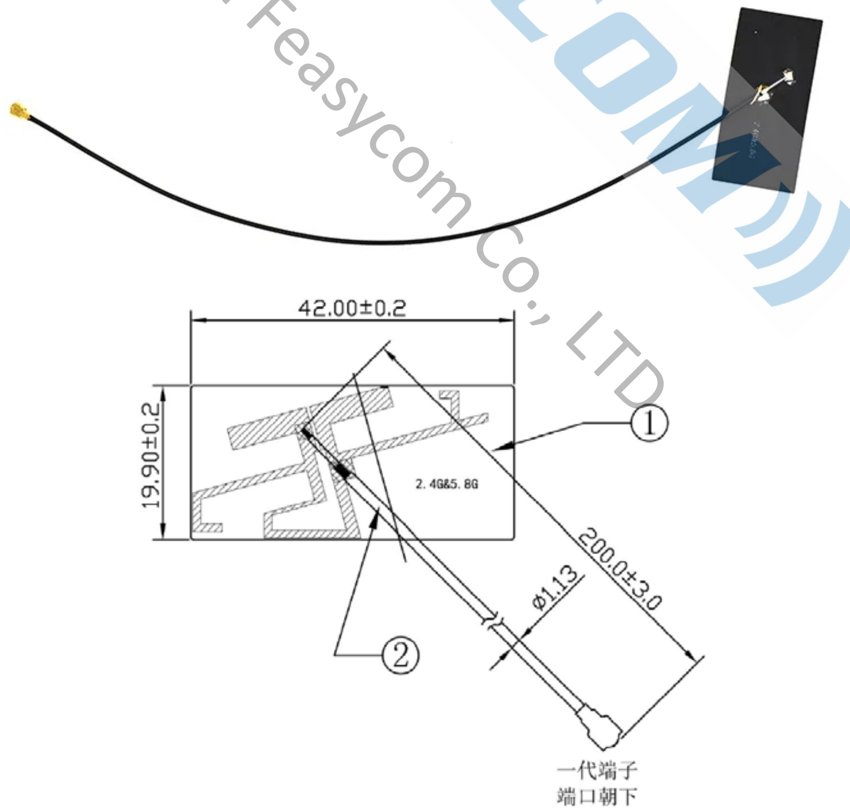

Figure 12-3-1: 2.4GHz & 5GHz Dual-band antenna, with IPEX first generation interface

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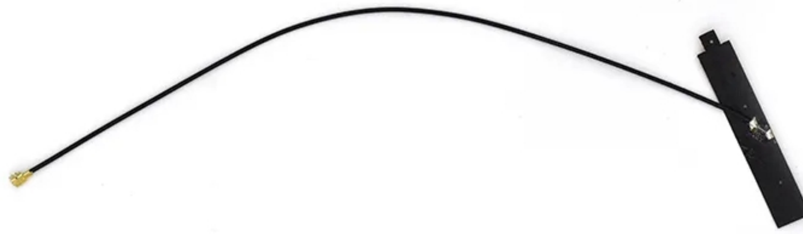

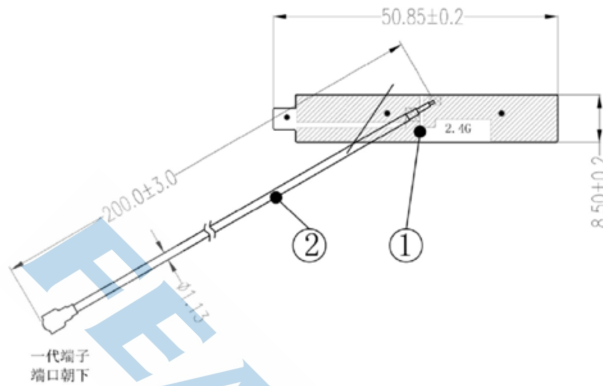

Figure 12-3-2: 2.4GHz antenna with IPEX first generation interface

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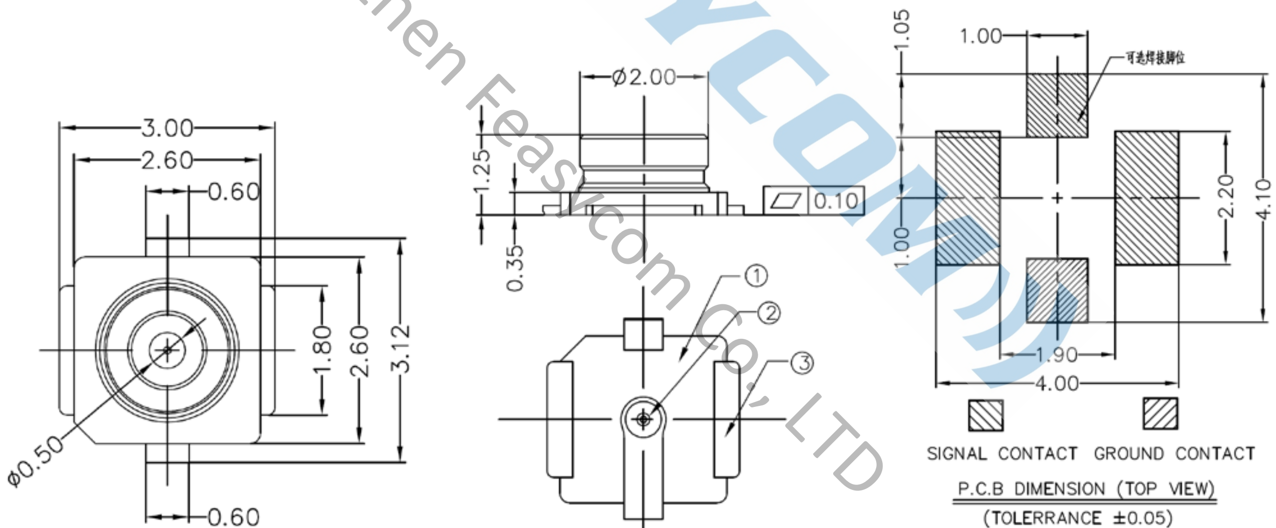

3	GROUND CONTACT	1	JIS C5191-H	Au 1u" Min. over Ni 50~100u" Min.
2	CONTACT	1	JIS C2680-1/4H	Au 1u" Min. over Ni 50~100u" Min.
1	HOUSING	1	LCP E6808	UL94V-0,30% GF
ITEM	NAME	Q'TY	MATERIAL ⚠	FINISH ⚠

NOTES:
1. FREQUENCY RANGE:
   DC TO 6GHZ (VSWR: 1.3MAX AT 0.1~3GHZ, 1.4MAX AT 3~6GHZ)
2. CHARACTERISTIC IMPEDANCE: 50 (NOMINAL);
3. TEMPERATURE: −40℃ TO +90℃;
4. RATED VOLTAGE : 60VAC;
5. CONTACT RESISTANCE :
   20m MAX.(SIGNAL CONTACT)
   20m MAX.(GROUND CONTACT)
6. WITHSTAND VOLTAGE : 200VAC FOR 1 MINUTE MIN;
7. INSULATION RESISTANCE : 500M MIN. AT 100VDC;
8. THIS COMPONENT IS HALOGEN FREE.

Figure 12-3-3: IPEX first generation interface

12.4 Soldering Recommendations

FSC-BW1001UV is compatible with the industrial standard reflow profile for Pb-free solders. The specific reflow profile used depends on many factors such as the thermal mass of the populated PCB, heat transfer efficiency of the oven and the type of solder paste used. It is advised to refer to the datasheet of the specific solder paste for profile configurations.

Feasycom provides the following recommendations for soldering the module to ensure reliable solder joints and proper module operation. However, since the optimal profile can vary based on the specific process and layout, these recommendations should be considered as a starting point guide and further study of the case is necessary.

12.5 Layout Guidelines (Internal Antenna)

Important Note: The antenna for FSC-BW1001UV is suggested to support both 2.4GHz and 5.8GHz dual frequency bands. We recommend using external FPC dual-band antennas instead of PCB onboard antennas. The following are general instructions for PCB onboard antennas for reference only.

It is strongly recommended to follow good layout practices in order to ensure proper operation of the module. Placing copper or any metal near the antenna can negatively impact its performance by affecting the matching properties. To prevent radiation, a metal shield should not be used with the module. It is advised to use grounding vias, spaced a maximum of 3 mm apart, at the edge of grounding areas to prevent RF penetration inside the PCB and unintentional resonator formation. Additionally, GND vias should be distributed all around the PCB edges.

In the restricted area where the on-board antenna is located, the motherboard should not have any bare conductors or vias. This area is not covered by stop mask print, so no copper (planes, traces, or vias) should be present in this area to avoid mismatching with the on-board antenna.

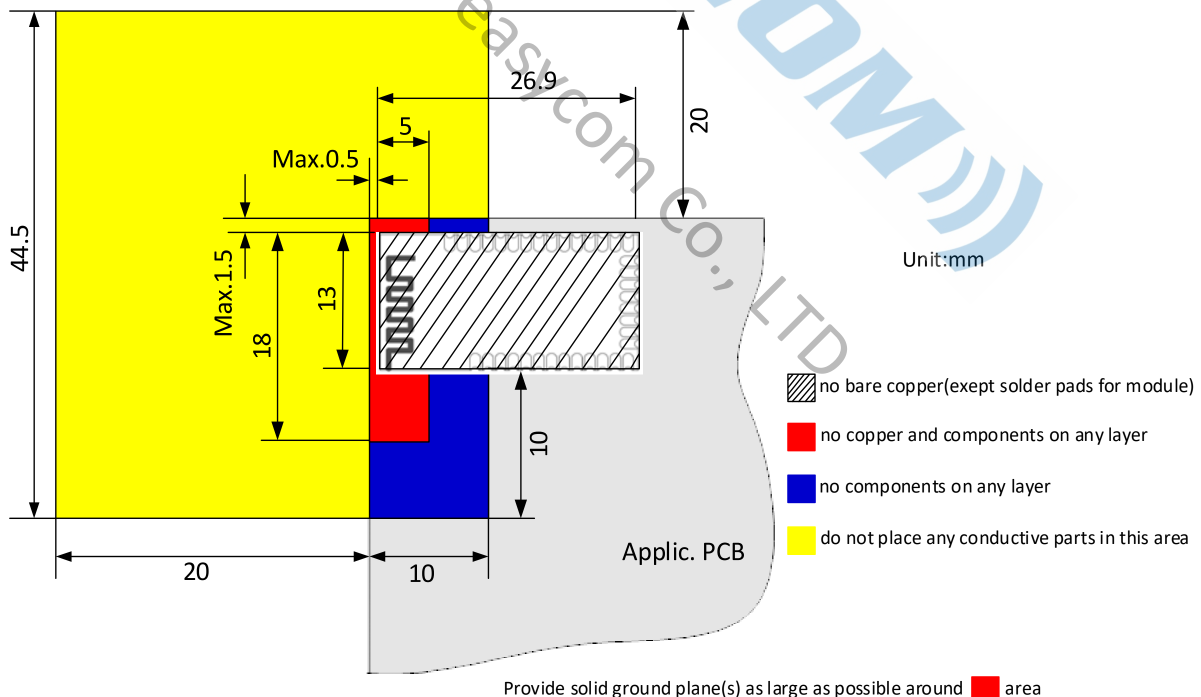

Figure 12-5-1：Restricted Area (Design schematic, for reference only.   Unit: mm)

The following recommendations are aimed at avoiding EMC problems caused by the RF part of the module. It is important to note that each design is unique, and this list does not cover all basic design rules, such as avoiding

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capacitive coupling between signal lines. Additionally, it is crucial to consider potential problems arising from digital signals in the design.

To mitigate EMC issues, it is advisable to ensure that signal lines have return paths that are as short as possible. For instance, if a signal passes through a via to an inner layer, always use ground vias around it. These ground vias should be located tightly and symmetrically around the signal vias. Routing of sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area both above and below the line. If this is not feasible, make sure to keep the return path short by employing alternative methods, such as placing a ground line next to the signal line.

12.6 Layout Guidelines(External Antenna)

The placement and PCB layout play a critical role in optimizing the performance of modules without on-board antenna designs. The trace connecting the antenna port of the module to an external antenna should have a characteristic impedance of 50Ω and should be kept as short as possible to prevent interference into the transceiver of the module. When positioning the external antenna and RF-IN port of the module, it is important to keep them away from any sources of noise and digital traces. To minimize return loss and achieve better impedance matching, a matching network may be required between the external antenna and RF-IN port.

To ensure proper RF performance, it is recommended to clearly separate the RF critical circuits of the module from any digital circuits on the system board. The RF circuits within the module are located near the antenna port. Therefore, the module should be placed in such a way that the module's digital part faces the digital section of the system PCB.

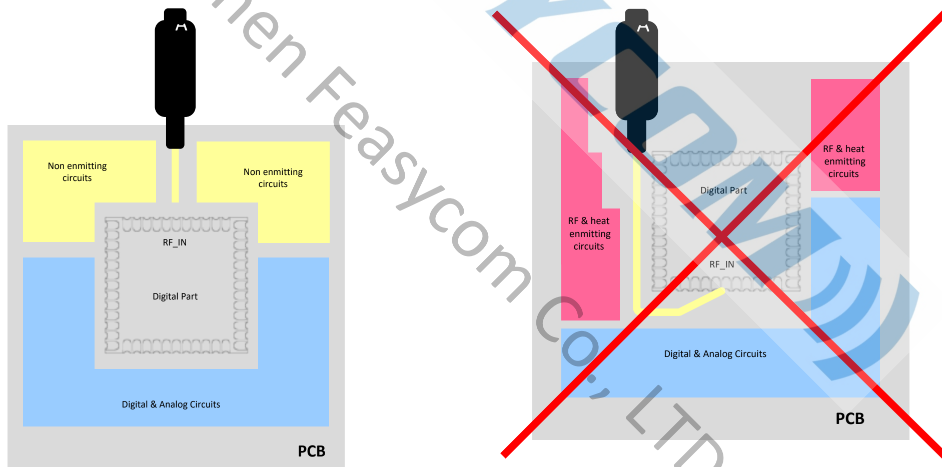

Figure 12-6-1: Placement the Module on a System Board

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12.6.1 Antenna Connection and Grounding Plane Design

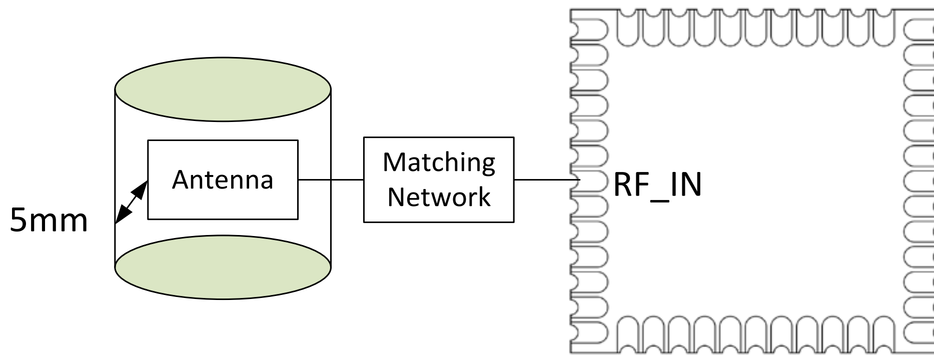

Figure 12-6-1-1: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

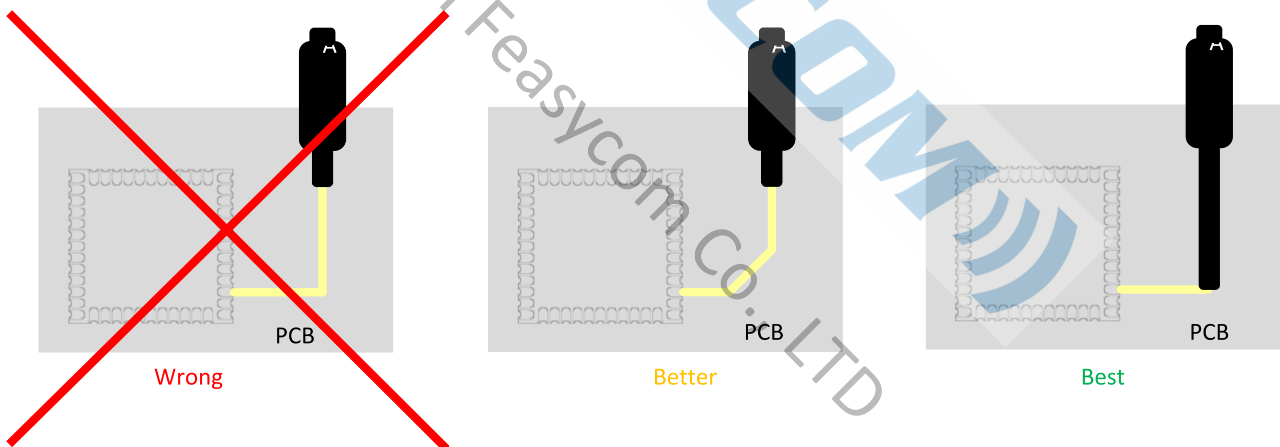

Figure 12-6-1-2: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

12.7 HCI Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 ~ 8mA

UART_RX

UART_TX

UART_CTS

UART_RTS

The route length of these signals be less than 15cm and the line impedance be less than 50Ω

12.8 Power Trace Lines Layout Guideline

VDD_1V8 Trace Width: 40mil

VDD_IO Trace Width: 20mil

12.9 Ground Lines Layout Guideline

A Complete Ground in Ground Layer.

Add Ground Through Holes to FSC-BW1001UV Module Ground Pads

Decoupling Capacitors close to FSC-BW1001UV Module Power and Ground Pads

13 PRODUCT PACKAGING INFORMATION

13.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 240mm * 185mm

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Figure 13-1-1: Vacuum Tray

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13.2 Packing box (Optional)

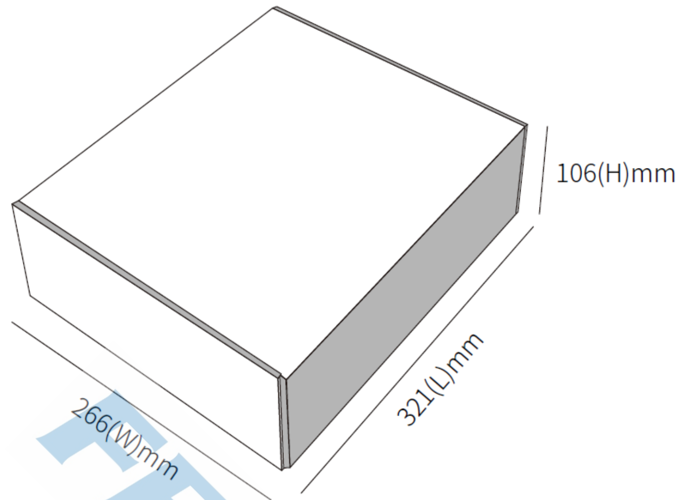

Figure 13-2-1: Packing box(Optional)

** If any packaging other than the package mentioned above is required, please confirm the packaging size again.*

** Packing: 1000pcs per carton (Minimum packing quantity).*

** The outer packing size provided above is for reference purposes only. For the actual dimensions of the product's packaging, please refer to the packaging of the actual goods.*

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14 APPLICATION SCHEMATIC

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